

# elektor

up-to-date electronics for lab and leisure

85

May 1982

65p.

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Rum - 78 Hz., ~



prop tacho

radio 3-2-1-FIRE

how BIASEd are tapes?

**ELEKTOR Artist:**  
the ultimate guitar preamp

Z-80 CPU Card

6502 housekeeper

**selektor****test tone generator**

How 'BIASED' are tapes? Although noise reduction and equalisation are necessary, the factor which contributes a considerable amount to the quality of recordings is correct application of 'bias'. In order to set this and match tape to recorder, a test tone generator as described in this article is required.

**the digital keyboard assembly and debounce circuitry****for the Polyformant**

U. Götz and R. Mester

As promised in the March issue, readers can commence building the Polyformant. The article is devoted to the practical side, starting with the debounce circuits for the keyboard contacts and the input unit.

**miniature MW receiver**

Using a well-proven chip, this article introduces a circuit with very few components, outperforming many commercially produced sets! In short a matchbox radio to set the world on fire.

**the Junior Computer as a frequency counter**

G. Sullivan

Microprocessors are often regarded as mathematical wizards. So why not use their aptitude for maths to the full and employ them also as a frequency counter?

**Z80-A-CPU card**

U. Götz and R. Mester

The Z80 is one of the most popular microprocessors around. It's about time the device was mentioned in Elektor. Although the Z80-A-CPU is the heart of the control unit for the new Polyformant, it is compatible with the Elektor bus system, therefore making the Eurocard collection accessible to Z80 users.

**the Elektor Artist**

It could be described as the ultimate in versatility for the electric guitar. This preamplifier (which can be used with any electronic instrument), provides a total of four inputs into two channels; extensive tone controls, built-in reverb and fuzz, with a large number of 'loop' switching facilities, giving the musician something at a reasonable cost which can only be found on more expensive equipment. We feel sure the Artist will satisfy constructors and discerning musicians alike.

**prop. tachometer**

A rev-counter for model aeroplanes. This design bridges the gap between the differing worlds of electronics and balsa wood. When matching a particular propeller to an engine a reliable method for measuring the rpm is extremely useful. The circuit described is straightforward in construction.

**6502 housekeeper**

Not just a clock but a sophisticated housekeeper based on the 6502 microprocessor. It can be used to control a multitude of household appliances, such as cookers, lighting, alarms, central heating. Set it weeks in advance and go on holiday without a care in the world.

**RAM/EPROM card for the Z80**

A. Seul

In principle the RAM/EPROM card (Elektor September 80) can be used with a variety of systems. Just a 'cut and shunt' exercise with no additional components is required to interface this card to the Z80 and more importantly to the Z80-A-CPU, as introduced elsewhere in this issue.

**software cruncher and puncher**

An unusual title perhaps, but one which succeeds in describing in as few words as possible what this article is about. a disassembler and EPROM programmer for the Junior Computer.

**market**

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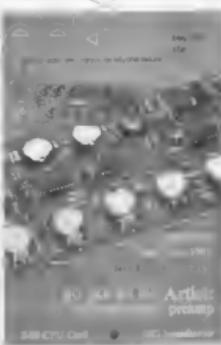
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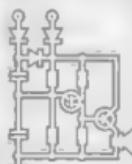
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**TV GAMES COMPUTER** — this book provides a different — and, in many ways, easier — approach to microprocessors. The TV games computer is dedicated to one specific task, as the name suggests. This provides an almost unique opportunity to have fun while learning!

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In this issue (the above prices include p. & p.)

# ELEKTOR BOOK SERVICE

# Selektor

## Photographing the hidden beauty of microchips

Manchester photographer Ad Sternberg is a man fascinated by the delicacy, beauty and colour of microchips. Combining highly sophisticated photographic and engineering techniques he has developed a unique method of photographing in fine detail and enlarging in full colour the integrated circuitry — invisible to the naked eye — of microchips, many little larger in diameter than the dot on a typewriter.

According to Mr. Sternberg, scientists and engineers in electronics have performed wonders in reducing them to a microcosm. A great deal of science and engineering skill is needed in photomicrography not only to produce a detailed negative image for enlargement but also enhanced and with controllable colour contrast.

Colour print examples of Mr. Sternberg's work in the photomicrography of microcircuits — enlarged possibly 400 times are now on display and used by internationally-known companies such as Plessey, Standard Telecommunications, International Computers, National Semiconductor and Ferranti Electronics. Mr. Sternberg's methods have been developed with special regard to photography of micro-circuits up to 8 mm (0.3 inches) diagonal, using a diffraction limited system.

Camels may not be able to go through the eye of a needle, microchips — which

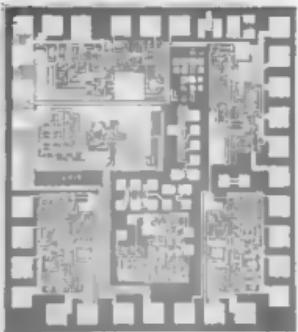


Photo 2. A typical Ferranti small integrated circuit photographed and enlarged by Ad Sternberg.

today provide the circuitry used in computers, space craft, rocket missiles, telecommunications and more humble objects such as cookers and washing machines — certainly can. Absolute cleanliness is vital. The tiniest particles of dust would produce big black blobs. Mr. Sternberg has been interested in photography since teenage. He joined an industrial and commercial photographic business in 1947, having previously spent some years learning to work to fine tolerances in an engineering tool factory. When silicon chips — microchips — arrived on the industrial scene in the 1960s he was approached by Ferranti who asked if he could, at reasonable cost, improve on the quality of the results they were getting themselves with colour photographs of silicon chips, wanted for publicity, record and internal company purposes. The biggest 'chips' were six millimetres square — others being much smaller.

Taking up the challenge, Mr. Sternberg found himself immersed in a year's experimentation and research. Little photographic material existed for this type of work, nor was there ready-made equipment. But, combining his photographic and engineering knowledge, he combed photographic, scientific instrument and second-hand shops for 'bits and pieces', and gradually designed his own equipment and techniques and colour processing methods.

A way of increasing the colour contrast had to be found. The colours in the microchips are very weak by the time they pass through the microscope optics. Correct lighting was a great problem. With high magnification, resolution figures can now be achieved that are better than one micron for small devices half a millimetre — around 20 thou — square, and better than four microns for large scale integrated chips, known as LSIs, over the whole field. The enlargement can be around 400 times.

The chips have become more complex,

of course, over the years. They pack more and more on one chip. Nowadays, computers have to be used to design the circuits because they are too complicated for even the finest scientists without computer aid. They have thousands of transistors and resistors on them. Mr. Sternberg believes, with good reason, that his equipment, methods and experience in this unusual field make his work unique — and that the techniques developed are applicable to photomicrography and photomacrophotography in general. Of course he realises there are other people in this field, particularly in the United States. However, it calls for quite a blend of different expertise not only in photography but also in engineering, optics and illumination — and dedication over a long period — to produce relatively low-cost results.

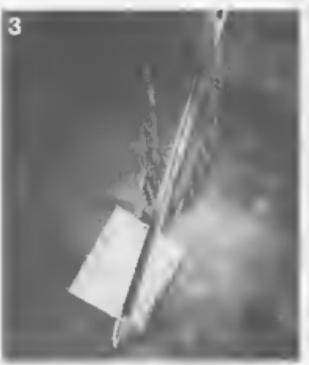


Photo 3. A Ferranti F100L microprocessor chip, containing approximately 10,000 transistors in the eye of a needle. The chip is about 1/5-inch square.



Photo 1. Ad Sternberg using a microscope to select a chip for photography.

## Televuchs Norwalk, Connecticut

The Maharaja Punkpin Bolanee has announced the formation of his Ethereal Television Network (ETV), marking the first of the so-called cultist organisations to enter the cable broadcasting industry. Claiming his programs will be patterned after those produced by the Christian Broadcasting Network, the Venerable One stated that the shows will attempt to 'cast light on the darkened corners of the cosmos, bringing peace and harmony to those seeking the Ultimate Truth and Karma'. The 146-year old mohatma said that ETV can currently be seen by 43,000 homes across the country and will be broadcast via the Comstar D-2 satellite thirty-six hours per week. Outlandish, you say? Perhaps, but not at all unlikely. According to a recent article in VideoPrint, it's just a matter of time!

*IRD Inc. USA*

# selektor

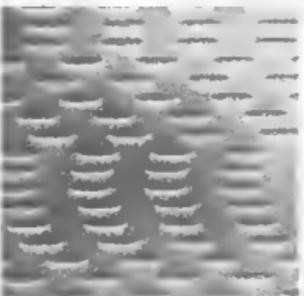
**LaserVision in the UK**

Philips intend to launch its LaserVision Disc system onto the UK market towards the end of May this year.

To start with, players and discs will be on sale in greater London and the surrounding home countries through a restricted number of outlets. These will include high street multiples, independent retailers and specialist rental companies. Philips plan to progressively increase the number of outlets into other major cities in the UK until distribution reaches a nationwide level at the earliest opportunity.

The first catalogue will contain more than 100 disc titles of which at least 75 will be in the shops by May. The remaining catalogue titles will become available shortly afterwards. Further new releases will substantially expand the catalogue by the end of the year. Seven top programme distributors will be marketing a wide range of titles on disc from the initial catalogue, including feature films, general entertainment programmes, musicals, sport and children's albums.

A strong advertising and promotional campaign has been set up with the intention of communicating the LaserVision message in an accurate and straightforward manner so that it may be understood at all levels of trade and by the consumers. LaserVision is a new and unique source of home entertainment and information for all the family. The easy-to-operate, damage-proof design of the player and the durable quality of the toughcoated discs allow the equipment to be used by everyone, even children.



Not only is Philips committed to developing the consumer market, but the company plans to enter the non-domestic market as well, as this offers considerable scope for the interactive application of LaserVision on the industrial, commercial and educational level.

1766 SI

## 250 kW Wind turbine

The need for alternative energy resources is not only a favourite discussion topic, but is at last leading to concrete results. Which of the elements (sun, sea or wind) is suitable for producing energy depends to a large extent on the local climate. Not surprisingly, solar energy can be found in abundance in deserts like the Sahara or in Arizona. Unfortunately, the British Isles do not have much sun to offer, but they are visited (and sometimes plagued) by plenty of sea breezes and gales, an inexhaustible source of fuel.

Wind energy projects are starting to be developed on an increasingly large scale, one of the most ambitious schemes to date being the wind turbine generator designed by the Wind Energy Group for

installation on Orkney. The Wind Energy Group comprises British Aerospace Dynamics Group, GEC Energy Systems Limited and Taylor Woodrow Construction Limited. The company has signed an agreement with the North of Scotland Hydro-Electric Board to construct the most powerful wind turbine generator ever built in the United Kingdom. It is to be erected on Burgr Hill, Orkney.

The 20 m diameter turbine has a rated power of 250 kilowatts (kW) at 17 metres/second (m/s) wind speed and a rotational speed of 88 revolutions/minute (rev/min). It will begin to operate at a wind speed of 8 m/s and shut down when wind speeds exceed 27 m/s. It has an estimated annual energy output of 700,000 kilowatt-hours (kWh). The machine is to have a synchronous generator, variable pitch rotor blade tips and a soft power transmission arrangement. Provision is being made for the machine to run in both fixed speed and variable speed modes. The rotor will be mounted to the main shaft with what is known as a teetering hub. This arrangement reduces the forces and moments on the blades and supporting structure.

The machine will be the first in the UK in recent times to be connected to an isolated diesel-electric grid system, and with a power rating of 250 kW will be the most powerful turbine to be connected in such a way anywhere in the world. These factors made its economic and technical evaluation especially relevant to many hundreds of similar grid systems elsewhere in the world who are burdened with large generating costs.

The Group has paid particular attention to this potential market in designing the transmission and control system of the machine to achieve power quality acceptable to a small diesel grid system. The prototype will allow for tests to evaluate fixed versus teetering hubs, constant versus variable speed operation, as well as a wide range of operational strategies. The machine is to be extensively monitored under a contract with the Department of Energy using a computer based data acquisition system which will scan sensors placed on the machine to measure performance, forces and displacements.

Procurement of components is now taking place prior to assembly and ground testing of the nacelle and rotor in the last quarter of 1982, while construction of the foundation and tower will begin in the summer. Commissioning and first synchronisation of the machine is scheduled for the first quarter of 1983.

The 250 kW machine also acts as the prototype for the larger machine which will be 60 m in diameter. When complete the project will be the largest demonstration in the UK of an alternative energy technology.



(1768 SI)

Certain cassette and reel-to-reel tape decks and recorders are equipped with such an array of meters and switches that some look as though they were intended for aircraft cockpits rather than for home use. Although noise reduction and equalisation circuits are necessary, the factor which contributes more than anything else to the quality of recordings is the correct application of 'BIAS'. In order to set the 'bias' correctly and therefore match recorder to tape, a signal generator, as described in this article is required. Armed with such a generator, readers are able to improve on the quality of recordings and use whatever tape type they wish.

# test tone generator



## how to set the 'BIAS' on your tape recorder

The existing range of decks and tapes is enormous. In an attempt to get over some of the confusion and conflicting sales literature, manufacturers tend to specify which type of tape will get the best performance out of their decks. This is fine, but no consideration is given in many cases to when the user can no longer afford, or get hold of the type of tape specified. Normally very little information is contained in the operating manual about altering the 'bias' setting, or even where to find the control.

Nearly all decks have equalisation circuits so that the record/playback signal reaching the preamplifier stage of a 'Hi Fi' system is as 'flat' as possible. Without such circuits the playback response would exhibit pronounced bass and treble losses. These losses are partly due to tape speed and type, but the bias also plays an important role. A correct 'bias' setting is needed to achieve a good recording level for all frequencies across the audio spectrum. This will in turn allow high playback output, low distortion, and a reasonably 'flat' response. Unfortunately there is a different ideal 'bias' setting for each frequency. The setting for a mid-frequency tone

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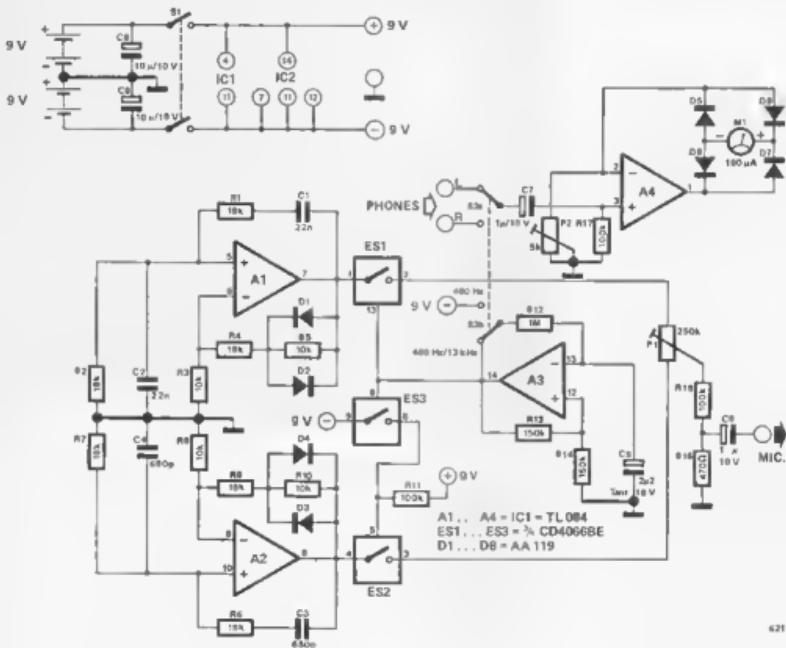


Figure 1. The circuit diagram of the complete tone generator and a suitable power supply circuit. Readers are advised to use 'Veroboard' as the construction medium.

(400 Hz) is quite different from the one required for a 13 kHz signal. Generally speaking, the higher the frequency the lower the 'bias' level. Therefore tape deck manufacturers specify the type of tape to use and choose a 'bias' setting (out of necessity) which is a compromise. A real in depth study of 'bias' is certainly not practical at this stage, as it would probably take up most of this issue. Anyway, we are more interested in practice than in theory.

### Tone generator

As outlined above a test tone generator supplying a mid and low frequency signal is necessary. Figure 1 shows the circuit diagram of the generator. It mainly consists of two bridge oscillators. The first one, arranged around A1, produces a practically distortion-free sine wave signal of 400 Hz. Stabilisation is achieved by using germanium diodes. The second oscillator (constructed around A2) operates in the same way, but produces a 13 kHz signal. Both signals are fed in turn to the output stage by means of the CMOS



switches ES1 and ES2. The circuit around A3 functions as a square wave generator with a frequency of about 0.25 Hz, activating the electronic switches in such a way that the output will alternate between 400 Hz and 13 kHz every two seconds.

With a positive pulse, ES1 and ES3 are closed and the 400 Hz signal reaches the output. With a negative going pulse ES1 and ES3 are open and ES2 is closed allowing the 13 kHz signal to be fed to the output. Preset P1 ensures the output amplitude for each signal is the same. The network made up of R15, R16 and C6, in the output stage, sets the impedance and level of output so that it can be fed directly to the 'mike' input of the deck.

The fourth opamp A4 is used to drive a dB level meter for monitoring purposes. A moving coil instrument or a multimeter set to the 100  $\mu$ A range is sufficient. Preset P2 sets the gain of A4. With the help of S2a the signal taken from the headphone socket of the deck can be monitored, one channel at a time. By switching over S2b the square wave generator is by-passed and only the 400 Hz signal reaches the output. Two completely separate switches can

be used for S2a and S2b. A single double-pole one was only used in the prototype for convenience.

### Checking and calibrating the test tone generator

Feed the output from the generator to both input channels of the tape deck. Turn the recording level controls of the deck to zero. If the deck has volume controls affecting the output level to the phones then turn these to zero as well. Centre P1 and P2, and switch on both the recorder and the generator. S2b is positioned to give a fixed 400 Hz signal. Now turn up the recording level controls until a reading of 0 dB appears on the 'vu' meters. Position S2b to activate the square wave generator part of the circuit. The frequency of the signal supplied to the recorder will fluctuate between 400 Hz and 13 kHz every two seconds. Rotate P1 until a balanced amplitude level for both frequencies is achieved, in other words, until the reading on the deck recording level meters is the same for both frequencies. With some recorders an amplitude drop will occur for the higher frequency. Should this happen then adjust P1 until the difference between the two readings is minimal, (say, 0 dB at 400 Hz and -3 dB at 13 kHz). Whatever the readings, take a note of them as they will come in handy later on.

Set the recording levels of the recorder to -20 dB and adjust P2 to give a monitor reading of 0 dB.

### Using the generator

Before going any further the following points should be kept in mind. Before adjusting the 'bias' give the



generator time to warm up.

Any procedures undertaken should be repeated several times in order to achieve reliable results.

Tape heads, etc. should be demagnetised and cleaned.

Insert a tape or cassette into the recorder, and record the 400 Hz and 13 kHz signals at a level of -20 dB and a monitor meter reading of 0 dB. Switch to playback and monitor the signals again for each channel and note if they are the same as the recorded ones. These should be approximately 0 dB or as previously noted (0 and -3 dB).

Any deviation in readings will mean that the 'bias' setting will have to be altered. Therefore, change this setting and repeat the procedures until the correct readings appear. The 'bias' setting will now be correct for the particular tape in use.

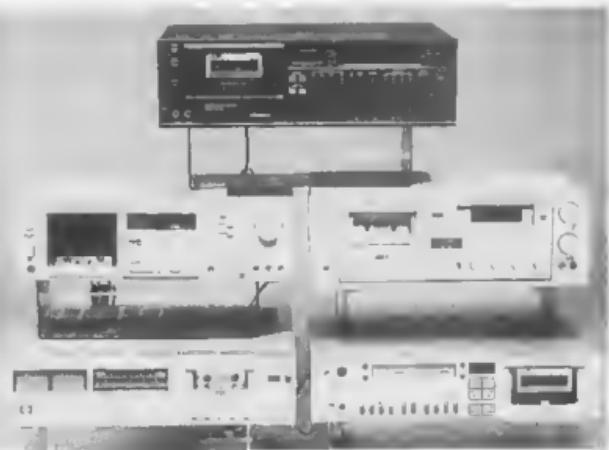
To set the 'Dolby' frequency roll-off level, first record only the 400 Hz tone,

after first disconnecting the monitoring circuit. It is advisable to check the manufacturer's instructions concerning the 'Dolby' settings before continuing. Switch to playback and note whether the playback level readings on the deck meters are the same as when the signals were recorded. If they are not then the 'Dolby' preset or control will have to be adjusted until they are.

That should now complete the procedures necessary to interface with the particular tape in question.

### Practical hints

Readers are reminded that the lower priced reel-to-reel and cassette recorders do not have an external 'bias' control. The lucky ones with middle and up-market models will certainly have these, making calibration far easier. For the unlucky ones it is best to consult a circuit diagram or other data in order to locate the presets inside the recorder. The 400 Hz tone is also very useful as a 'bench-mark' in the calibration of 'equalisation' and other audio circuits.



# polyphonic synthesiser

U. Götz und R. Mester

## the digital keyboard assembly and debounce circuitry

The general principles and basic theory behind the new Elektor polyphonic synthesiser were introduced in the March 1982 issue. However, this article is devoted to the practical side, namely the constructional details, thereby enabling readers to commence building. We start off with the debounce circuitry for the keyboard contacts and the input unit (together with its bus board) which acts as the keyboard interface for the main CPU card.



Photo 1. This photo shows how the debounce unit, the input unit, the tune-shift unit and the bus board are mounted and wired.

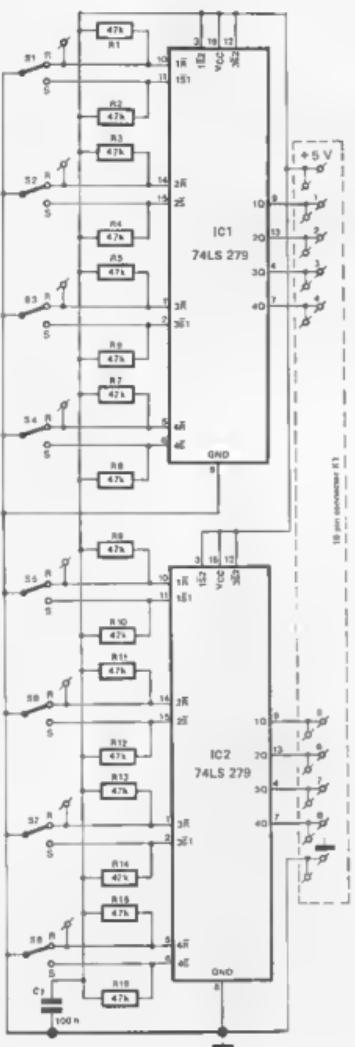
The digital keyboard design caters for up to five octaves (61 keys). Although it is obviously possible to use fewer keys, the relatively small price difference between three and five octave keyboards prompted the designers to go for the latter. This also means that the range of musical possibilities can be exploited to the full. The keyboard contact blocks, or switches, are mounted on eight individual printed circuit boards in seven groups of eight and one group of four. Each board also contains the debounce circuitry for its respective keys. The contact blocks used are the (gold wire) single pole GJ type from Kimber Allen. The debounce circuitry for each key consists of an RS flipflop. There are ten connections between each printed circuit board and the input unit, 8 for the debounce circuitry and 2 for the power supply.

By now, readers will have noticed that only half of the eighth printed circuit board is used, meaning that only 60 of the 61 keys can be used (see figure 8). A close examination of the debounce circuitry in figure 1 and the printed circuit board layouts in figures 5, 6 and 7 should provide a clue, however. Effectively, the 8 printed circuit boards are identical. The 8 keys on each board are subdivided into two groups of four. The reason for this is that the design had to fulfil the main conditions of optimum performance and value for money, while being simple to construct. In reality, the keys at the extreme ends of the keyboard are very rarely used anyway. If readers wish to use the lower key rather than the higher one, all that needs to be done is to shift the connections down one key (or semitone). This does not present too much of a problem, since the VCOs of the individual channels can be adjusted to give the required pitch. If all 61 keys are to be used, then the 8th printed circuit board will have to be fully utilised. This does mean, however, that the printed circuit board assemblies would protrude from the side of the keyboard, making it more difficult to fit the unit into a case. To make construction easier and for space considerations, we suggest that the last board is cut in two and the unused half discarded (see figure 8). This means, of course, that the relevant connections on the input board will have to be grounded. In practice, this is accomplished by earthing the four respective pins on the ten-pin connector. If this was not carried out, the processor would be confused into thinking that the non-existing keys were permanently depressed!

### Mechanical construction

The keyboard contact blocks are mounted on the underside of the board (see figure 3). Position the blocks (notch side towards the board) on the printed circuit board and glue them into place. A good strong adhesive such as Araldite

1



Key contacts: Kimber Allen Typ GJ

82106-1

Figure 1. The keyboard debounce circuitry.

should be used. The adhesive should be applied sparingly taking care not to get any near the contact wires. Bend the short wires at the rear of the blocks towards the board and solder them into place. It is important to remember that the contact blocks must be wired so that the circuit is closed when the key is depressed.

The next step is to drill a hole in a convenient place near the centre of each printed circuit board. This hole should be large enough to allow a self-tapping screw and the blade of a screwdriver to pass through it. The reason for this is so that the carrier board can be mounted directly to the keyboard chassis (this is explained later on).

All the other components, including the 10 pin connector, are then mounted on the boards. The 8 (17% actually) boards are now ready to be assembled on to the carrier board, by means of suitable nuts, bolts and spacers. The length of the spacers should not exceed the overall height of the contact blocks, which is approximately 9.5 mm with the types specified.

The carrier board is then attached to the keyboard chassis. The spacing between the carrier board and the chassis is very important. The key push rods are often in 'fishplate' form (see figure 2) so as to allow the centre contact spring to be located in one of the holes. It is essential that the centre contact spring touches the upper contact when the key is depressed.

Most keyboard chassis' are not pre-drilled, therefore readers must decide for themselves where the carrier board is to be attached. Self-tapping screws are ideal for this operation, which brings us back to the holes previously drilled in the centre of the printed circuit boards. The latter will help to stabilise the construction considerably.

Exact dimensions and sizes for the carrier board, case and so on cannot be given, as these will depend on the type of keyboard used.

### Testing the debounce circuitry

The debounce circuitry can be tested quite simply. The two power supply connections on the 10 pin connector (of one printed circuit board) are linked to +5V and ground respectively. When a key is released, the voltage at the corresponding debounced output should be zero volts. This should rise to +5V when the key is depressed. If all is well the keyboard can be put to one side for the time being. Take care not to damage the contact wires, since they are very fragile and will bend very easily.

### Input unit

The input unit shown in figure 3 consists basically of an 8 bit data bus over which the processor is able to read in

2

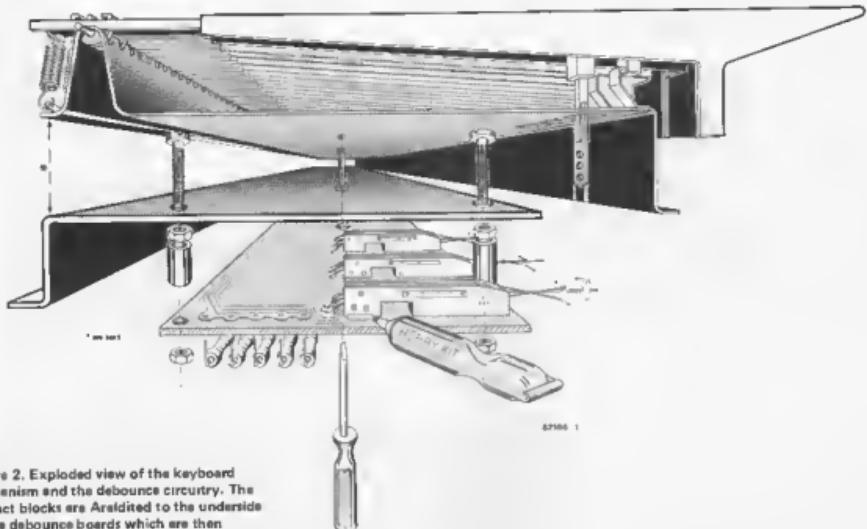


Figure 2. Exploded view of the keyboard mechanism and the debounce circuitry. The contact blocks are soldered to the underside of the debounce boards which are then mounted on a 'carrier' board.

3

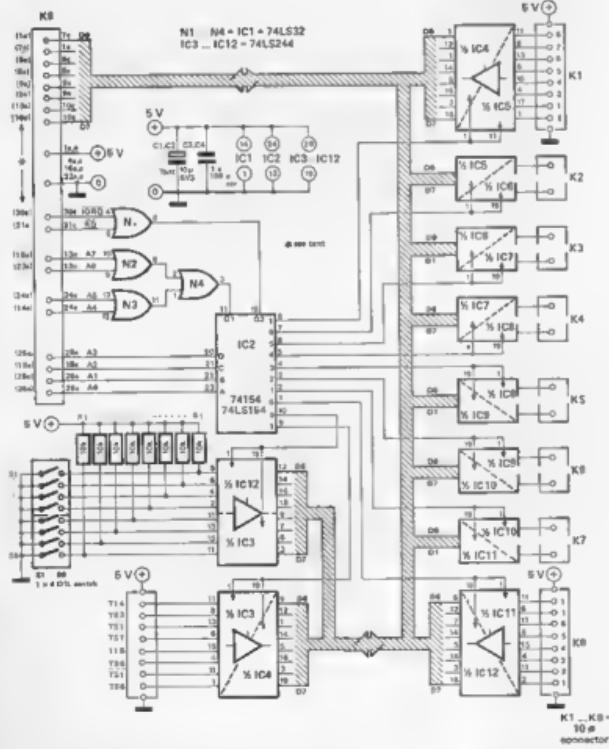


Figure 3. The circuit diagram of the input unit.

data (by means of multiplexing) via the buffer stages, IC3...IC12. The outputs of these buffers are held in a high impedance state until such time as the devices are enabled by means of the signal presented to pins 1 and 19.

Address lines A0...A7 originate from the microprocessor and are decoded via gates N1...N4 and IC2 to produce the select signals for the data buffers. This means that only one data buffer will be enabled at a time and the processor will always 'know' exactly which one is being addressed.

As the data and address lines are common to both the input and the output units, the input data will have to be disabled when the output unit is being accessed. This is accomplished by gating the RD and T0RQ signals from the microprocessor and feeding the resultant signal to one of the select inputs of IC2.

The construction of digital data processing systems can be kept simple and small, by using a common highway for multiple data transfer (this is a typical procedure in computer systems). It is interesting to know what the data presented to the microprocessor looks like. The inputs of the majority of the buffer ICs are connected to the outputs of the debounce circuitry. The processor scans the buffer ICs one by one by means of the chip enable inputs (pins 1 and 19) so that it can determine exactly which, if any, key is being depressed.

The buffer consisting of half of IC3 and half of IC12 is used by the microprocessor to determine the number of VCOs which are available in the synthesiser. As mentioned previously, any

number of VCQs between 2 and 10 can be incorporated. The eight DIL switches, S1 . . . S8 are used to preset this number according to the information given in table 1.

The connections TS1...TS8 lead to the 'tune-shift' board, which is shown in figure 4. A diode matrix ensures that the correct logic levels are presented to the data bus when switch S1 is operated. In this way the VCO frequencies can be transposed by one octave, one semi-tone at a time. Three pushbutton switches, S2...S4, connected to the tune shift circuit determine the 'direction' in which the notes are shifted. The logic levels required by the system software are presented to the data bus via connections TS5 and TS6. Of the four possible set/reset latches contained in IC1, only three are used to effectively 'decode' the state of the three switches (latches 1, 2 and 4). Under normal conditions, S3 will have been depressed and the output of the first latch (1Q) will be high whereas the outputs of the other two (2Q and 4Q) will be low. Now, if S2 is depressed, the output of the second latch (2Q) will go high and the other two latches will be reset via gates N2 and N3. Similarly, if S4 is depressed, output 4Q goes high and latches 1 and 2 are reset via gates N1 and N2. Gates N1 and N3 are used to reset latches 2 and 4 when switch S3 is depressed. The current 'state of affairs' is indicated by the three LEDs (D21...D23) connected to the latch outputs via inverters N4...N6. These LEDs are mounted inside the switches. The remaining latch in IC1 (latch 3) may be used in the future for expanding the keyboard.

The CPU card and the output unit with its corresponding digital-to-analogue (D/A) conversion system will be described in subsequent articles.

Table 1

The coding for switches S<sub>1</sub> ... S<sub>8</sub>:

The setting for switches S1 . . . S8 indicates the number of available oscillators in binary. Switch S5 (bit 4) indicates the presence/absence of the preset facility. For the time being, switches S6 . . . S8 (bits b5 . . . b7) are ignored by the processor.

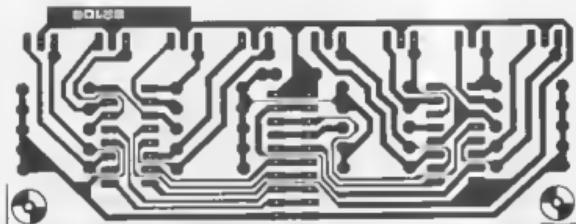
switch number	S8	S7	S6	S5	S4	S3	S2	S1
bit value:	b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	0
	0	0	0	0	0	1	0	0
	0	0	0	1	1	0	1	1
	0	1	0	0	0	0	1	0
	0	1	0	0	1	0	0	1
	0	1	1	0	0	1	1	0
	0	1	1	1	0	1	1	1
	1	0	0	0	0	0	0	0
	1	0	0	1	0	0	0	1
	1	0	1	0	0	0	1	0
	1	1	0	0	0	0	0	0
	1	1	0	0	0	1	0	0
	1	1	1	0	0	0	0	0
	1	1	1	1	0	0	0	0
	1	1	1	1	1	0	0	0
	0	x	x	x	x	x	x	x
	1	-	-	-	-	-	-	-

Table 2

#### Coding of the data at the tune-shift output:

bit value	b7	b6	b5	b4	b3	b2	b1	b0	
	0	0	x	x	x	x	x	-1 octave	
	0	1	x	x	x	x	x	0 octave	
1	0	x	x	x	x	x	x	+1 octave	
1	1	x	x	x	x	x	x	not valid	
	x	x	0	0	0	0	0	0 semi-tone	
	x	x	0	0	0	0	1	+1 semi-tone	
	x	x	0	0	0	1	0	+2 semi-tone	
	x	x	0	0	0	1	1	+3 semi-tone	
	x	x	0	0	1	0	0	+4 semi-tone	
	x	x	0	1	0	1	0	+5 semi-tone	
	x	x	0	1	1	0	0	+6 semi-tone	
	x	x	0	1	1	1	1	+7 semi-tone	
	x	x	1	0	0	0	0	+8 semi-tone	
	x	x	1	0	0	0	1	+9 semi-tone	
	x	x	1	0	0	1	0	+10 semi-tone	
	x	x	1	0	1	1	1	+11 semi-tone	
	x	x	1	1	0	0	0	not valid	
	x	x	1	1	0	1	0	not valid	
	x	x	1	1	1	0	0	not valid	

5



## Parts list for figures 1 and 5

## Resistors:

 $R1 \dots R16 = 47\text{ k}$ 

## Capacitors:

 $C1 = 100\text{n}$  ceramic or MKT

## Semiconductors:

 $IC1, IC2 = 74LS279$ 

## Miscellaneous:

8 key contacts (Kimber Allan (gold wire)/  
type GJ/single pole)

10 pin plug (Molex male E 3022-10A)

10 pin socket (Molex female E 3071-10)

10 crimp terminals (Molex 4809 CL)

Note: all of the above are required eight times

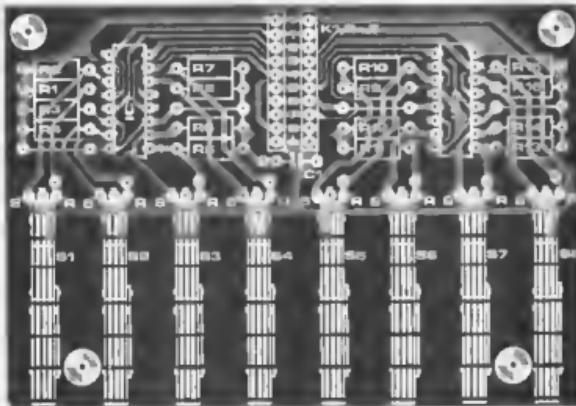


Figure 5. The printed circuit board and component overlay of the debounce unit.

## Parts list for figures 3 and 6

## Resistors:

 $R1 \dots R10 = 10\text{ k}$ 

## Capacitors:

 $C1 = 10\mu/6.3\text{ V}$  tantalum $C2 \dots C4 = 100\text{n}$  ceramic or MKT

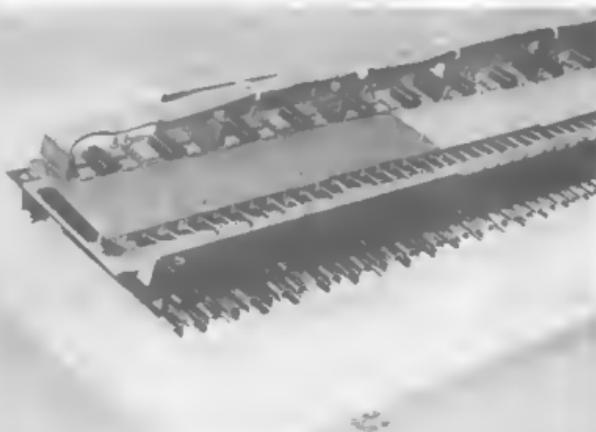
## Semiconductors:

 $IC1 = 74LS32$  $IC2 = 74LS154$  $IC3 \dots IC12 = 74LS244$ 

## Miscellaneous:

S1 ... S8 = 2 x 4 way DIL switches  
9 ten-pin plugs and sockets and  
crimp terminals (see parts list for  
the debounce unit)

angled 2 x 32 way plug (DIN 41612)



## Parts list for figures 4 and 7

## Resistors:

 $R1, R2 = 1\text{ k}$  $R5 \dots R10, R14, R15 = 10\text{ k}$  $R11 \dots R13 = 470\Omega$ 

## Capacitors:

 $C1, C2 = 100\text{n}$  ceramic or MKT $C3 = 1\mu/6.3\text{ V}$  tantalum

## Semiconductors:

 $D1 \dots D20 = 1N4148$  $D21 \dots D23 = 3\text{ mm red LED}$   
(in digitast switches S2 - S4) $IC1 = 74LS279$  $IC2 = 74LS02$  $IC3 = 74LS14$ 

## Miscellaneous:

S1 = single pole 12 way rotary switch

S2 ... S4 = digitast (with LEDs)

10 way plug, socket and crimp terminals  
(see parts list for debounce unit)

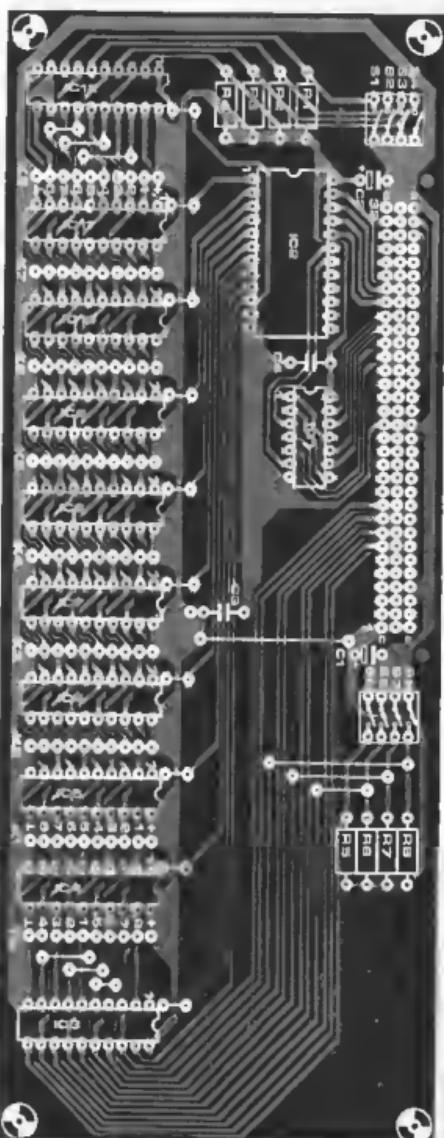
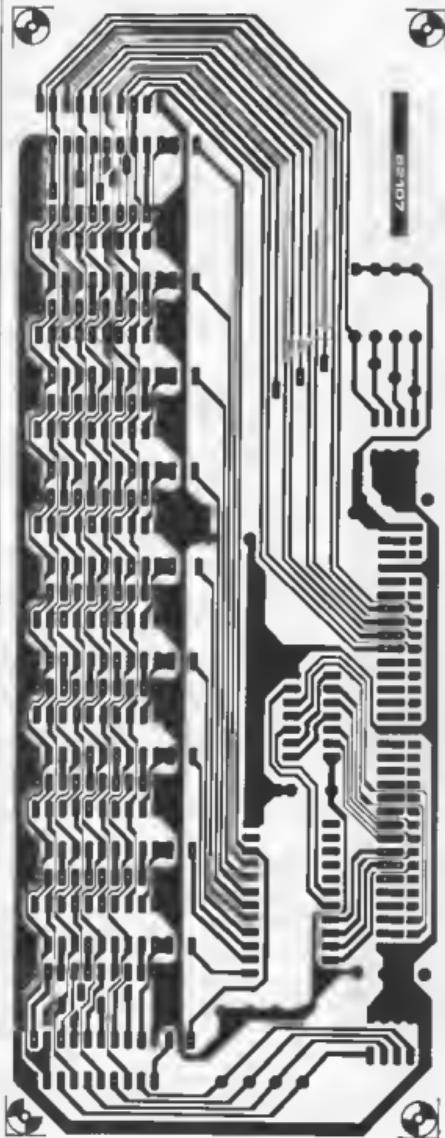


Figure 6. The printed circuit board and component overlay of the input unit.

7

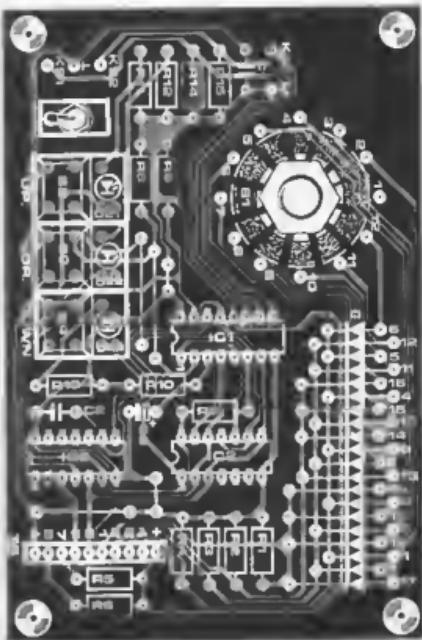
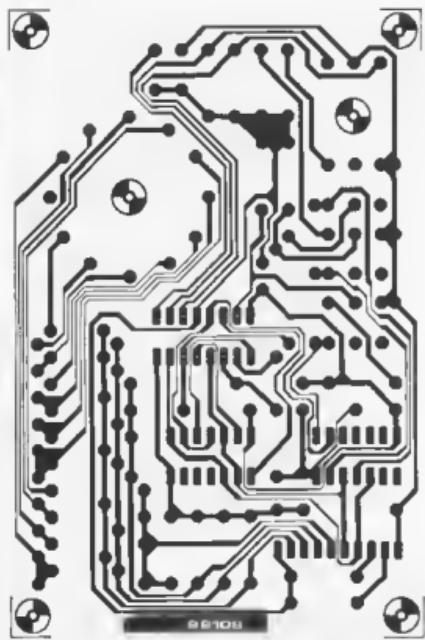


Figure 7. The printed circuit board and component overlay of the 'tune-shift' unit.

8

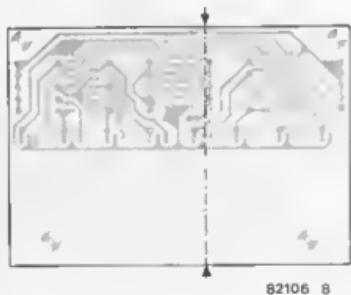


Figure 8. A section of figure 5 showing where the 8th debounce board can be sawn in two without damaging the copper tracks.

The system has been designed such that the existing Elektor bus board (EPS number 80024) can be used to link the CPU card and the input/output units. A suitable method of mounting the various parts of the system are shown in the photograph. ■

The design is based on the MW receiver circuit which was published in March 1981. This circuit lends itself very well to miniaturisation because it requires very few components and the power consumption (0.3 mA) is sufficiently low to allow the use of a small mercury cell.

The Ferranti ZN 414 IC is the 'heart' of the circuit. This IC is reasonably well known by now; its 3 pin housing containing a straight through receiver. The only external components required are the tuning capacitor and aerial. Figure 1 shows a block diagram of the IC; a high impedance input stage, an RF amplifier, an AM detector and an AGC (automatic

gain control). Readers wishing to know more about the inner workings of the ZN 414 are referred to the March 1981 issue of Elektor.

Figure 2a shows the circuit diagram of the complete receiver, when a high resistance (approximately  $200\ \Omega$ ) magnetic earpiece is used. The simplicity of construction is more akin to crystal set design than anything else. The resistance of the earpiece is very important, since this controls the gain of the IC and therefore the output volume. An earpiece with an internal resistance (not to be confused with impedance) of around  $200\ \Omega$  is ideal, but types having a lower resistance (within reason) can also be used, together with a resistor ( $R_x$ ) connected in series. Readers should take note not to use too high a value for  $R_x$ , otherwise the output will be rather poor. Obviously the sensitivity of the earpiece will also have a bearing. The absolute minimum resistance ( $R_x +$  earpiece) is about  $100\ \Omega$  with the maximum being  $1k5$ . A good compromise is about  $500\ \Omega$ . The prototype actually used an earpiece of  $170\ \Omega$  together with a resistor of  $330\ \Omega$ . If the value of  $R_x$  is high, then the connection of an electrolytic capacitor, in parallel (not more than  $10\ \mu F$ ) should improve the output level. The actual value is not critical and will depend on the  $R_x$ /earpiece combination. Basically readers are invited to find the com-

# miniature MW receiver

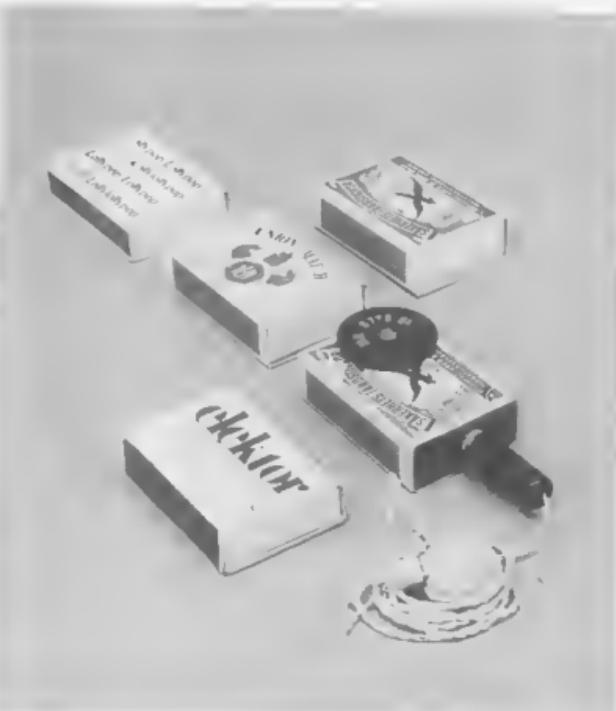
a matchbox radio to set the world on fire . . . ?

Over the past fifty years a lot of miniature radio circuits have been designed. Unfortunately most of them have suffered from a lack of output power and sensitivity.

Furthermore the majority always had problems with the aerial.

Readers may remember the wrist watch type radios that came to the fore some time ago, when an aerial had to be wound around the wrist or in the strap. Anyway, very few of them gave a worthwhile performance.

With the advent of the ZN 414, designs became simpler and better. Using this well-proven chip, the article introduces a straightforward circuit with very few components which can outperform many equivalent commercially produced sets. It has good output power, reception and selectivity.



1

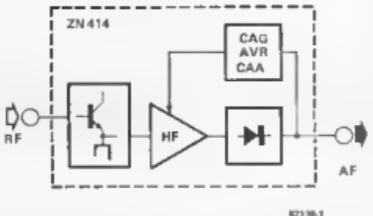


Figure 1. The block diagram of the interior of the ZN 414. This tiny IC forms the basis of the matchbox receiver.

2

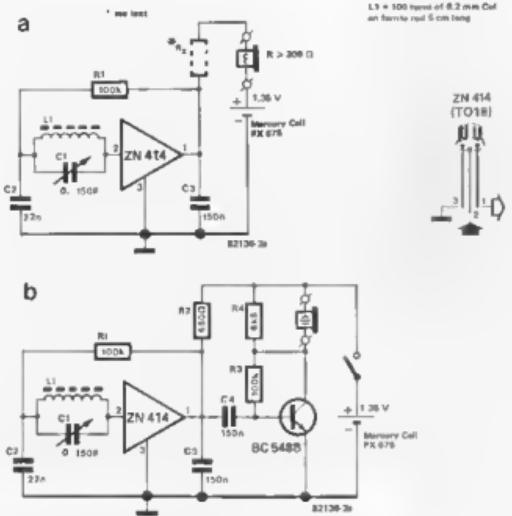


Figure 2. The basic circuit (a) uses a high impedance magnetic earpiece. An output stage is required if a crystal earpiece is to be used (b).

3

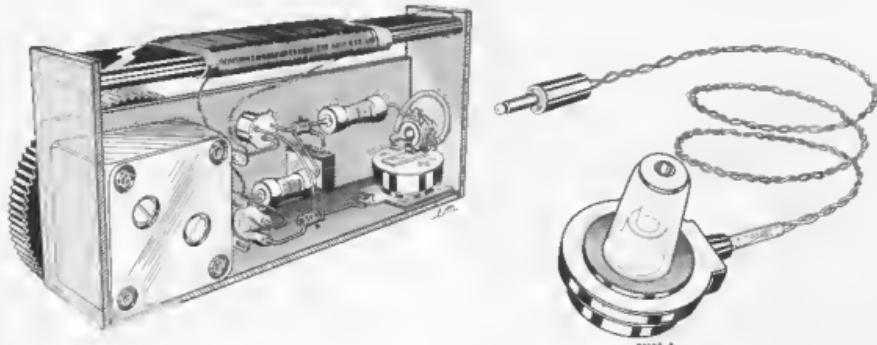


Figure 3. The construction of the matchbox radio is illustrated here. The 'chassis' is made from plastic sheet and fits inside a matchbox. There is plenty of room for all the components including the output stage if required.

bination applicable to their needs, as it really depends on what output level is required.

Unfortunately the frequently used  $8\ \Omega$  type is not suitable as it requires the addition of a matching transformer. A high impedance crystal earpiece on the other hand, requires an additional output stage, as shown in figure 2b. The power consumption in both circuits (2a & 2b) is practically the same, because the additional stage (figure 2b) only adds an extra 0.1 mA drain on the battery.

A decoupling capacitor for the power supply is not required, since the internal resistance of the mercury cell is extremely low.

### Construction

The choice of housing is left to the reader as it will depend on the size of the components. The prototype was inserted into a matchbox (see photo) simply as a guide-line and to give an impression of its relatively small size. The original design has a flat ferrite rod, 50 mm in length with a cross-section of 12 x 4 mm, but any rod approximately 10 mm in diameter will suffice. The aerial coil is made up of 100 turns of 0.2 mm enamelled copper wire, wound onto a paper or cardboard former. The ferrite rod is inserted into it. The variable capacitor is one of the twin-ganged variety (141 pF and 59 pF) commonly used by manufacturers in commercially available medium wave pocket radios. Should readers wish to have a lower number of windings or use a ferrite rod with an unusual permeability factor, they are advised to connect both gangs in parallel.

As everyone will agree, to design a printed circuit board for this radio would be futile, as that would probably take up more space than the complete



radio. It is more convenient to interconnect the components directly. Figure 3 shows one method for this. The 'chassis' is made of plastic having the same dimensions as the 'tray' of a matchbox. The variable capacitor is mounted onto the chassis by means of appropriate screws. The ferrite rod is attached by glueing each end to the sides of the chassis.

A standard earphone socket is used. Normally the switch part acts to isolate the loudspeaker, but in this case it is utilised as a battery connection. The moving contact part of the switch is cut off with pliers or a wire cutter to leave only the fixed terminal. This serves as the positive contact for the battery. A small brass plate (glued to the side of the chassis) serves as the negative contact. The position of the socket is determined by the size (width) of the better.

Note that an on/off switch is not necessary when constructing the circuit as in figure 2a. The supply is automatically switched on when the earpiece is plugged in. However, the circuit as in figure 2b does require a switch.

The battery should be a mercury type cell such as a 'Mallory' supplying 1.35 V.

### Final remarks

A whine or whistle heard in the earpiece when tuning between stations can be eliminated by swapping over the connections to the aerial coil. Normal mercury cells are able to deliver 200 mAh, so each cell should give between 400 and 500 hours of listening pleasure. ■

# the Junior Computer as a frequency counter

G. Sullivan

**Microprocessor systems are often regarded as mathematical wizards, so the Junior Computer's aptitude as a frequency counter will come as no surprise . . .**

As the name suggests a 'frequency counter' records a recurrent series of events. This does not necessarily have to be anything to do with electronics. The merry month of May, for instance, (and any other month, for that matter) has a frequency of one sunset every 24 hours (although it isn't often seen in the British Isles). To take an electronic example, if an AC voltage changes its polarity one hundred times per second, this is referred to as a frequency of 50 Hz.

The point is, by what criteria is frequency measured? In the second example the number of polarity changes (from positive to negative, or vice versa) that occur during one second are simply counted. When a microprocessor is

'hired' to do the calculation work, e program consecutively displays the contents of three display buffers, in other words the last frequency to be measured. The program is interrupted either once the one second measuring time has passed, or the AC voltage has gone low. A new program is now run to check the cause of the interrupt. If a zero-crossing was involved, the period counter is incremented by one. But if the measuring time (1 second) has passed, the contents of the counter memory locations are copied into the display buffers. At the same time, a new measuring period begins. At the end of the process, a return is made to the main routine, after which the whole procedure starts all over again.

1



B2126.1

Figure 1. A series of interrupts (IRQ) are required for frequency measurement.

2

```

$1A00 A9 B6 INITPR LDAM $0B
$1A02 85 D8 STAZ ACCUL
$1A04 85 D1 STAZ ACCUM
$1A06 85 D2 STAZ ACCUH
$1A08 A9 29 LDAM IRQSRV
$1A0A BD 7E 1A STA INQL
$1A0D A9 1A LDAM IRQSRV/256
$1A0F BD 7F 1A STA INQH
$1A12 BD 86 1A STA EXITG
$1A15 A9 10 LDAM $1B (1610)
$1A17 85 D4 STAZ TIMER
$1A19 85 D3 STAZ COUNT
$1A1B A9 3D LDAM $3D (6110)
$1A1D 85 D5 STAZ TIMEH
$1A1F BD 7F 1A STA CNTH
$1A22 58 CLI
$1A23 20 B6 1D LOOP JSR SCANDS
$1A26 4C 23 1A J.J LOOP
$1A29 4B IRQSRV PHA
$1A2A 5A TZA
$1A2B 4B PHA
$1A2D 9B TYA
$1A2D 4B PHA
$1A2E 2C D5 1A BIT RFLAG
$1A31 10 1C RPL ADD
$1A33 A5 D5 LDAM TIMEL
$1A35 BD 7F 1A STA CNTH
$1A38 06 D3 DECO COUNT
$1A3A D0 2B BNE EXIT
$1A3C A2 02 LDIM $B2
$1A3E A8 02 LDIM $B0
$1A4B 85 D8 STORE LDAM ACCUL,X
$1A42 95 F9 STAZ INH,X
$1A44 94 D8 STZE ACCUL,X
$1A46 CA DEK
$1A47 10 F7 RPL STORE
$1A49 A5 D4 LDAM TIMEH
$1A4B 85 D3 STAZ COUNT
$1A4D D6 15 BNE EXIT
$1A4F FB ADD SED
$1A50 1B CIC
$1A51 A5 D0 LDZ ACCUL
$1A53 69 B1 ALDIN $B1
$1A55 85 D8 STAZ ACCUL
$1A57 A5 D1 LDZ ACCUM
$1A59 69 B8 ALDIN $B8
$1A5B 85 D1 STAZ ACCUM
$1A5D A5 D2 LDZ ACCUR
$1A5F 69 B8 ALDIN $B8
$1A61 85 D2 STAZ ACCUH
$1A63 D8 CLD
$1A64 68 EXIT PLA
$1A65 A8 TAY
$1A66 68 PLA
$1A67 AA TAX
$1A68 68 PLA
$1A69 4B RTI

```

## ADDITIONAL ZERO PAGE LOCATIONS

ACCOL	\$0003
ACCUM	\$0001
ACCUH	\$0002
COUNT	\$0003
TIMEH	\$0004
TIMEL	\$0005

N1,N2 = 1/3 IC1 = 4049

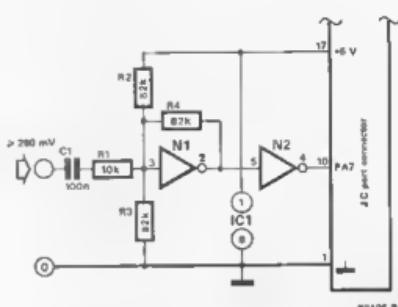


Figure 2. This circuit is added to the Junior Computer to effect the program in figure 1.

The events are depicted in the flow chart in figura 1.

A certain amount of hardware is also needed and this is shown in figura 2. This circuit is connected to the port connector of the Junior Computer to allow the frequency data to be entered into the computer. A significant negative zero-crossing in the input signal will pull port line PA7 low. The program makes sure this is accompanied by an IRO.

The software is provided in the table. The start address of the program is \$1A00. When data is written into location EDETC, PA7 is pulled low thereby enabling an IRQ. Preparations include defining the IRO jump vector at the start address of the IROSRV interrupt routine, starting the interval timer (CNTH, in other words, an IRO is enabled after every 1024 clock pulses) and storing the contents of location COUNT. Then the program LOOP is run until an IRQ takes place.

As soon as any type of IRO is detected, the IROSRV program is run. After saving the A, X and Y contents (used during SCANDS) on the stack, the computer examines the N flag. If N, or rather the timer flag, is zero, the IRO cannot have been enabled by a time out. This means that it must have been caused by a change in logic level on PA7. A new AC voltage period has passed and so the computer proceeds to label ADD. The 24-bit BCD number (ACCUH, ACCUM, ACCUL – the period counter in figure 1) is incremented by one. After restoring A, X and Y (EXIT) and executing an RTI, the computer returns to LOOP.

Supposing the IRQ was caused by a time out in the interval timer. The timer is started afresh and the contents of COUNT are decremented by one. Provided COUNT has not yet reached

zero, a jump will be made to EXIT. If, however, COUNT is in fact zero, the STORE section is run. The measuring period has now passed and the display buffers, POINTH, PQINTL and INH, are assigned values equal to those of ACCUH, ACCUM and ACCUL, respectively.

So much for the program, let's put everything into practice. Connect the circuit in figure 2 to the port connector, enter the program on the keyboard (or even better, read it in from cassette) and start it via the main JC keyboard. (The main JC keyboard must be used, so as to provide the I/O definition for SCANDS.) The highest frequency that can be measured is about 10 kHz. At low frequencies greater accuracy may be obtained by extending the measuring time to 10 seconds (load A0 instead of 10 into TIMEH, address \$1A16). The result on display will of course have to be divided by ten to give the correct frequency.

Literature:  
Chapter 6 of the Junior Computer Book II.



Table 1. The frequency counter program.

Considering the amount of brain power stored away inside the Z80-A, the CPU card circuit is surprisingly straightforward. As can be seen from figure 1 all that is needed to make the brain tick is a handful of ICs. Memory is organised according to the Elektor systems' page structure, in other words, it consists of 4K blocks. The first block (0000...0FFF) is located on the CPU board and contains 2K of EPROM (0000...07FF) and 2K of RAM (0800...0FFF). This particular board was designed for use with the new polyphonic synthesiser or Polyformant and the combination is described in detail elsewhere in this issue. Since only 1K

formant requires a Z80-A (MK 3880-4) CPU.

Essentially, the operating speed of the processor mainly determines the time it takes to execute a program. In the Polyformant, the CPU must scan the keyboard and in the extended version it must also scan all the presets. Furthermore, it must pass on all the relevant data to the Polyformant modules (VCOs, VCFs and so on). How much time these processes take depends on the response speed of the microcomputer. This is particularly important when the keyboard is being scanned. The faster the scan, the sooner a VCO will be able to react to a depressed key. Using the software package developed for the Polyformant, a VCO can respond within two or three milliseconds. This delay is far too short to be noticeable.

# Z80-A CPU card

... for the Polyformant

As the Z80 is still one of the most popular microprocessors around, it is high time the device was mentioned in Elektor. However, that is not the only motive behind this article, for the Z80-A CPU is the heart of the control circuitry for the new Elektor synthesiser. The board is compatible with the Elektor microprocessor bus system, so that the Eurocard collection will now be accessible to Z80 users.

of RAM is required in this application IC18 and IC19 (see figure 1) may be omitted.

It is not absolutely necessary to position the memory ICs and their corresponding address decoders on the CPU board. Large amounts of software can best be stored on a separate EPROM board, such as the Elektor RAM/EPROM card (ESS 80120). One or two minor modifications to the latter are required first, however, details of which are provided elsewhere in this issue.

## Buffers

Any self-respecting CPU board will of course have to be properly buffered, as the CPU outputs are unable to drive a complete system directly. Since the buffers used here (IC9...IC13) are tri-state and are enabled by the BUSAK signal, the DMA, or multiprocessing, facility of the Z80 is retained.

## Speed

The processor is driven by a 4 MHz crystal oscillator. This is the highest possible clock frequency for a Z80-A or MK 3880-4 CPU. With the standard Z80 or MK 3880 the clock frequency should not exceed 2.5 MHz. It should be mentioned at this stage that the Poly-

## Wait cycles

The use of a high clock frequency automatically calls for corresponding processing speeds, or access times. The access time of a standard 2716 EPROM (IC15) will usually be too long for it to be addressed by the CPU. As for date entry, even less time is available for writing to the RAMs (IC16...IC19).

There are two ways in which this problem can be solved. The first method involves the use of high-speed memory devices, that is to say, EPROMs and RAMs with an access time of 350 ns and 250 ns, respectively. The latter are easily obtainable nowadays, but 350 ns EPROMs are a little harder to find. Strictly speaking, even 350 ns is 'cutting it a bit fine', although a shortcut may be taken by implementing the OE (output enable) input instead of the CE (chip enable) input. This enables a 350 ns 2716 to be used without the need for any special measures.

The other alternative is to slow down the CPU and use normal 'low-speed' EPROMs. This is done by adding wait cycles to read operations. A wait cycle lasts exactly one clock period, that is, 250 ns. The addition of a single wait cycle will therefore extend the EPROM access time to 500 ns, which gives plenty of leeway to even the most 'sluggish' types. The delay is effected by including flipflops FF1 and FF2 in the circuit.

The flipflops are only active while the EPROM (IC15) is being addressed (the D input of FF2 is low). They may be omitted if a 350 ns EPROM is available, in which case a wire link, J1 must be included instead of IC4. This deactivates the delay circuit. When testing the CPU, however, readers are advised to carry out the first method initially and include a wait cycle, so as to be absolutely sure that a slow EPROM will not complicate matters.

Any external memory or peripheral devices are also able to generate wait cycles by way of the WAITEX input.

U. Götz and R. Mester

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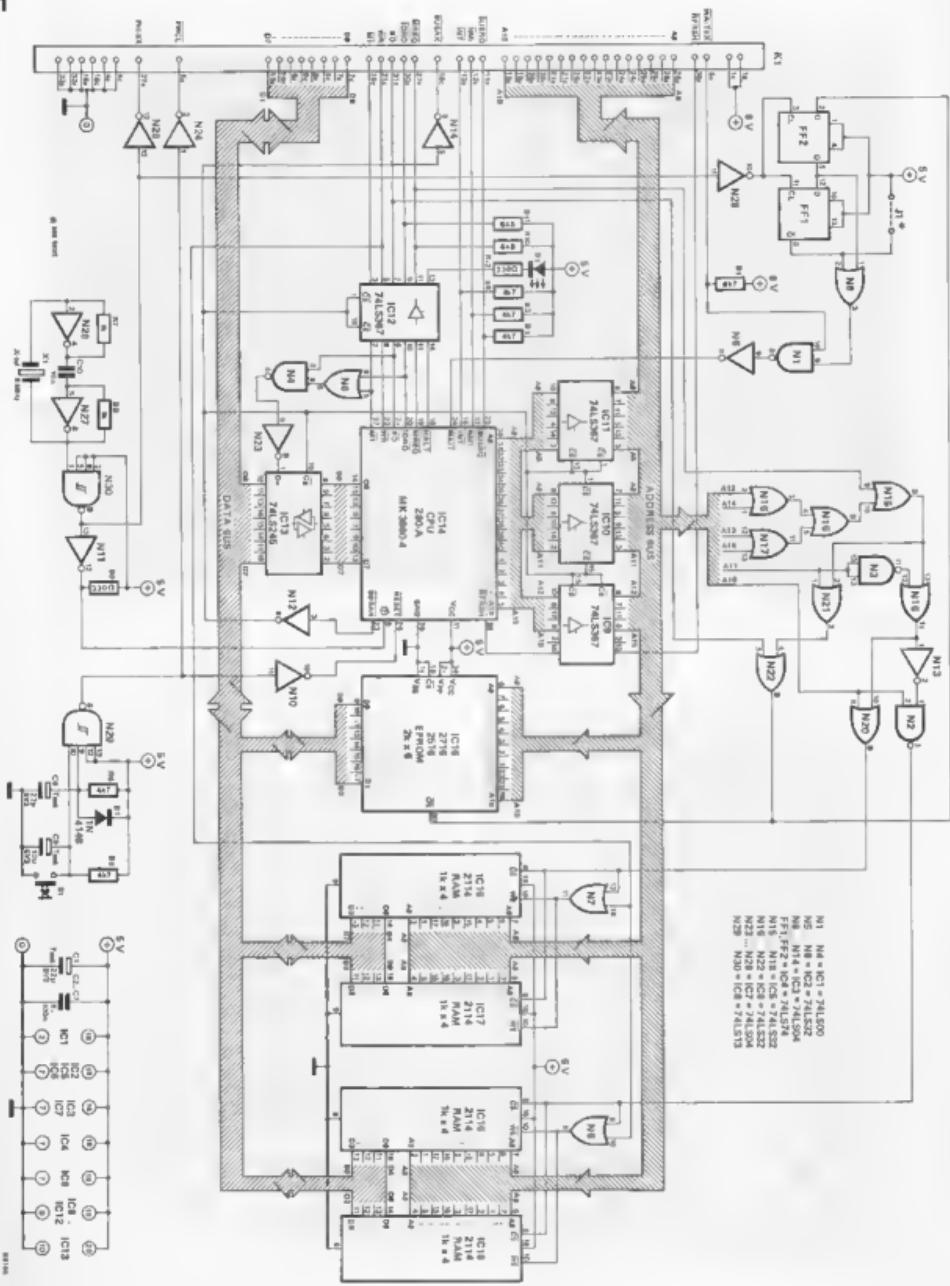


Figure 1. The circuit diagram of the Z80-A CPU card.

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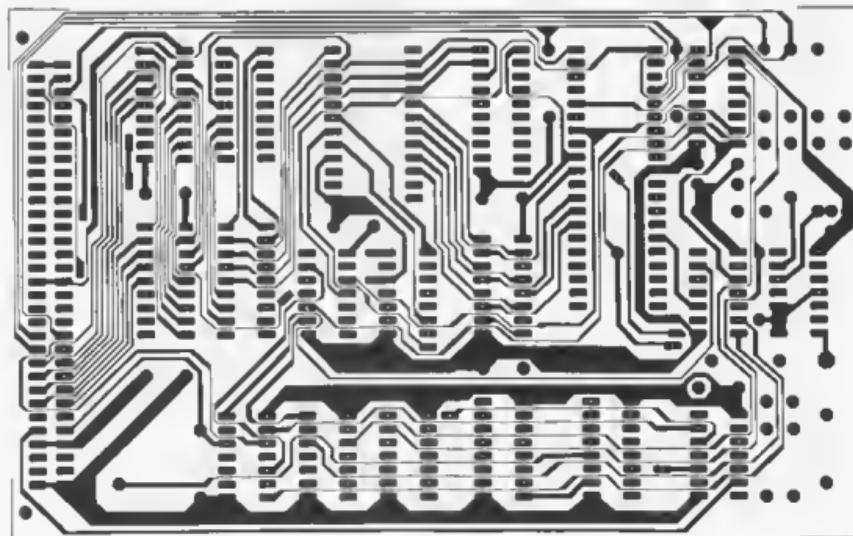
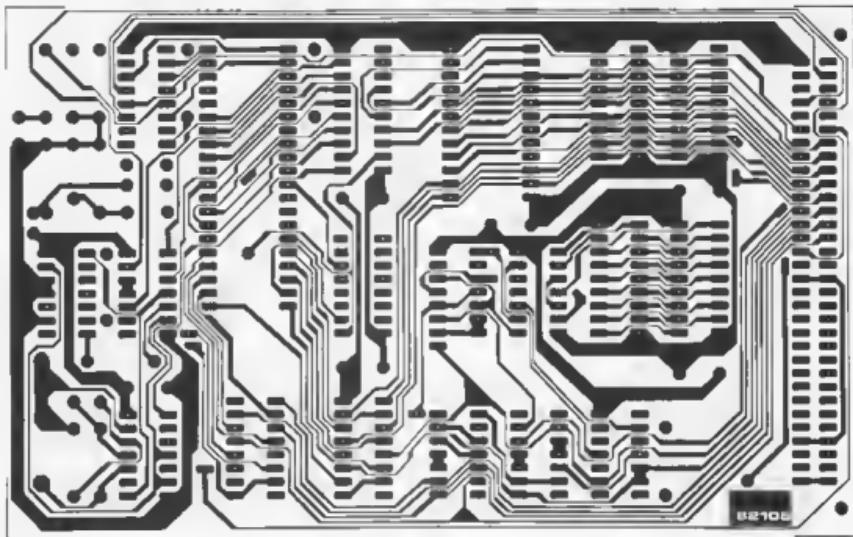


Figure 2. The copper track pattern for the double sided printed circuit board.

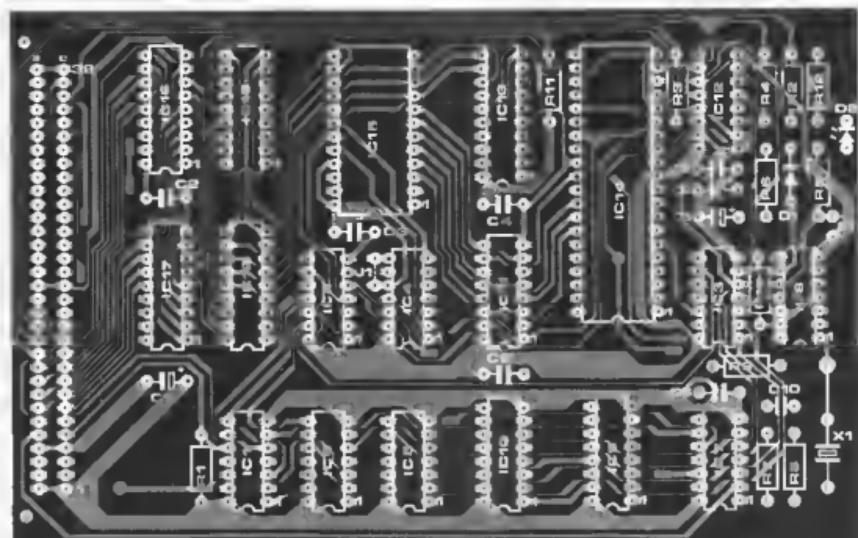


Figure 3. The component overlay for the Z80-A CPU card

**Parts List****Resistors**

R1 . . . R6 = 4k7  
R7, R8 = 1 k  
R9 = 330 Ω  
R10, R11 = 6k8  
R12 = 470 Ω

**Capacitors:**

C1 . . . C7 = 22 μF/6.3 V tantalum  
C8 . . . C7 = 100 nF ceramic or MKH  
C9 = 10 μF/6.3 V tantalum  
C10 = 10 nF MKH

**Semiconductors:**

D1 = 1N4148  
D2 = LED  
IC1 = 74LS00  
IC2, IC5, IC6 = 75LS32  
IC3, IC7 = 74LS04  
IC4 = 74LS74  
IC8 = 74LS13  
IC9 . . . IC12 = 74LS367  
IC13 = 74LS245  
IC14 = Z80-A (or MK3880 4)  
IC15 = 2716/2516  
IC16 . . . IC19 = 2114 Z or 2114A-5  
(access time 250 ns)

**Miscellaneous:**

S1 = push button switch  
X1 = 4 MHz crystal  
K1 = 64-pin connector

**Reset**

Reset circuitry is needed to initialise the CPU. When the power supply is switched on, R6, C8 and D1 hold the reset input of the CPU low for a while via N29 and N10. This is the PWCL signal and serves to reset any other boards connected to the system bus. An external reset facility has been provided for emergencies. It is advisable to place S1 'out of reach' to prevent it from being inadvertently depressed thus causing valuable information to be irrevocably lost.

**The printed circuit board**

Apart from S1, all the components in figure 1 are mounted on a Eurocard sized, double-sided, plated-through printed circuit board. This is shown in figure 2. As the pin assignment of the 64-pin connector corresponds to that of the Elektor bus system, the board may be used in combination with a number of existing cards.

The components should be mounted on the CPU card with due care, because in some places on the board the copper tracks are so close to each other that soldering may easily cause a 'short'. Although the board is provided with a solder mask to reduce this sort of problem, a great deal of care is still required.

**Further information on the Z80**

Enough has been written about the Z80 to fill an entire library. Plenty of software is available too, but users must be well-informed of the requirements of their particular system. Often the software has to be adapted for specific purposes and this does call for a fair amount of expertise. The CPU board published here was designed for the Polyformant and a special article is devoted to its use with the synthesiser. A brief description of the software is also given.

The Polyformant is, of course, just one application possibility out of thousands. The advantage of using the board in a different system is that the hardware can be adapted to existing software packages. Such modifications are usually left up to the user, but nine times out of ten it is much easier to rearrange computer circuitry than to re-write programs.

Elsewhere in this issue an article describes how to modify the 8K RAM + 2K EPROM card for use with the Z80 and therefore how readers can create their 'own' computer system.

# the Elektor Artist

## a versatile electric guitar preamplifier

This preamplifier is a companion to the 100 W power amplifier published in the April 1982 issue of Elektor. Two independent channels are provided each with two inputs. Features include high end low impedance inputs, extensive tone controls, built-in reverb and fuzz and effect 'loop' switching, providing the musician with all the extras normally found on the more expensive equipment at a reasonable price. Although originally designed for the guitarist, it can of course, be used with any other electronic instrument such as an organ or synthesiser.

Designing a really good circuit for a guitar preamplifier was quite a challenge. After a considerable number of requests from Elektor readers our design staff set about creating the Artist. The primary objective was to produce a preamplifier that satisfied a discerning musician while still remaining a practical proposition for home construction. All the Artist's effects are combined onto a single printed circuit board, thereby simplifying construction considerably. The advantages of the switching modes will be obvious to the adventurous musician. This facility is something that musicians are always looking for, but rarely finding in commercial equipment, with the possible exception of HH.

The front panel layout in figure 4 is a good point from which to start describing the circuit and facilities. It is basically a twin channel preamplifier having a low and high input. Channel I includes a five band graphic type tone control circuit, built-in Fuzz and Reverb. The amount of distortion can be fully controlled and ranges from a 'clean' to extremely 'dirty' sound. By-passing the Fuzz circuit does not result in any noticeable change in output volume.

Channel II has a simpler parametric type of tone control and reverb. The reverb 'loop' can be patched into both channels, independently or simultaneously. The Fuzz circuit is only available on channel I.

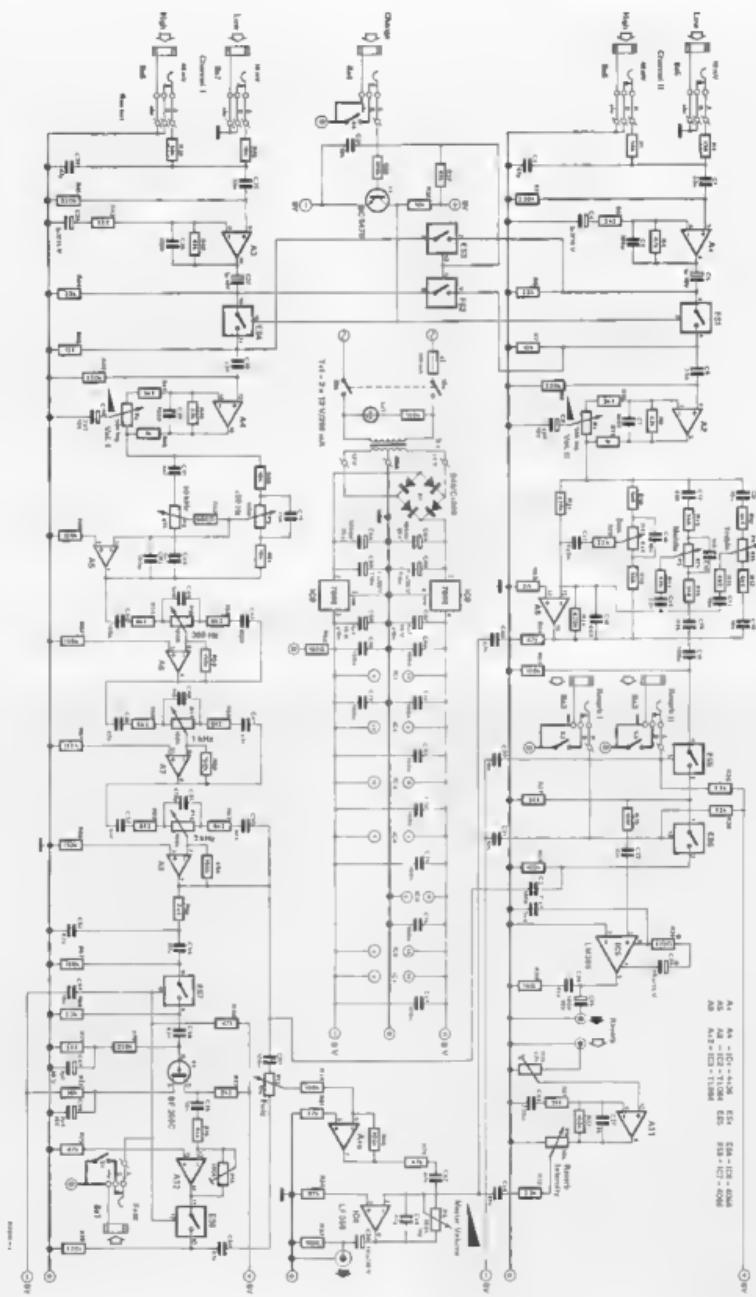
A switch enables an input to be fed to either of the two channels. This allows the player to preset both channels and switch from one to the other at will. The channel change facility as well as the 'effect' switching can be remote controlled by means of foot switches. Finally, input volume controls and a master volume potentiometer complete the circuit.

### The circuit

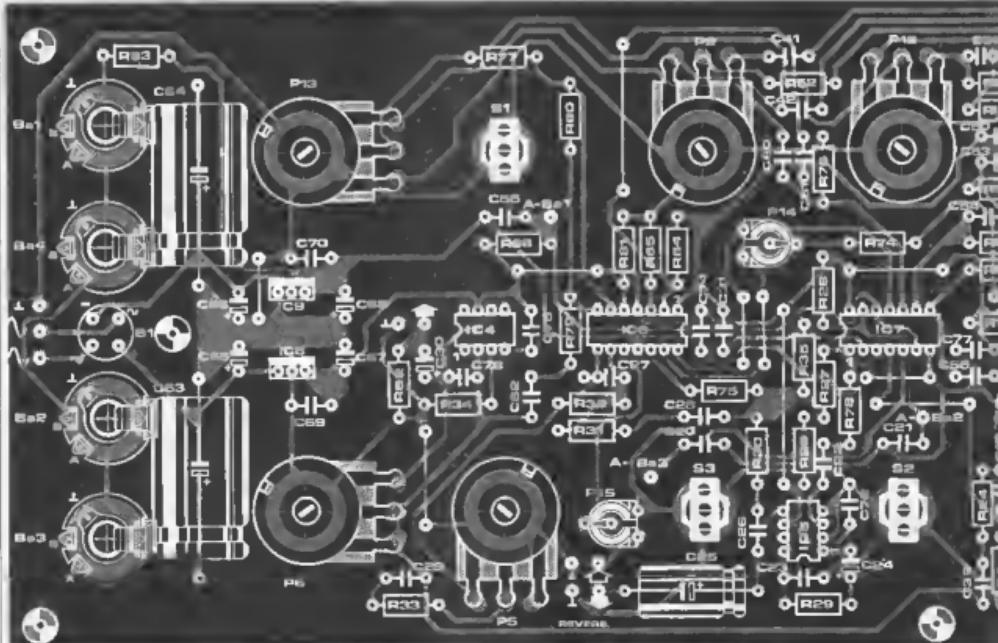
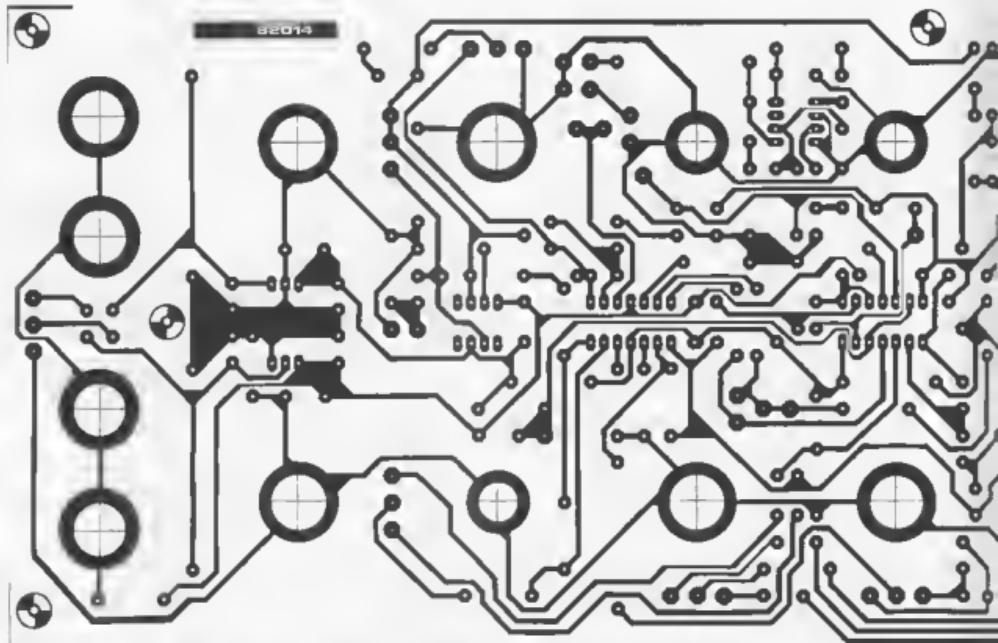
Figure 1 shows the circuit diagram of the 'Artist'. CMOS analogue switches have been used instead of FET power transistors. This helps to keep the overall cost down without impairing quality. The input signal from sockets Ba5 ... Ba8 is fed to the non-inverting inputs of A1 and A3 (IC1), via the resistor network R1, R2, R39, R40. These set the sensitivity of the input (tailoring it to any guitar), and ensure

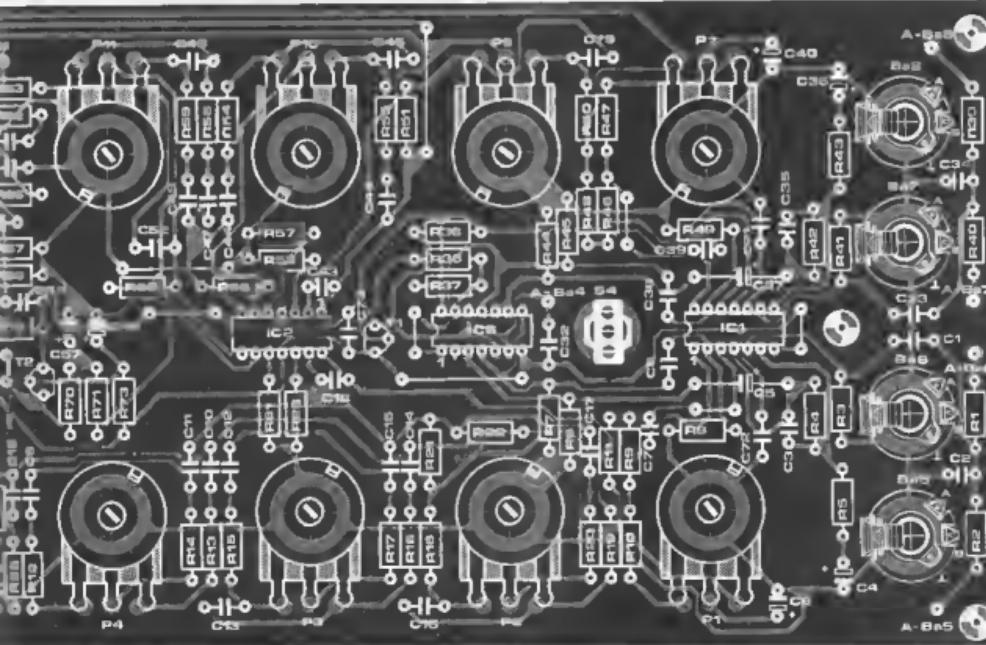
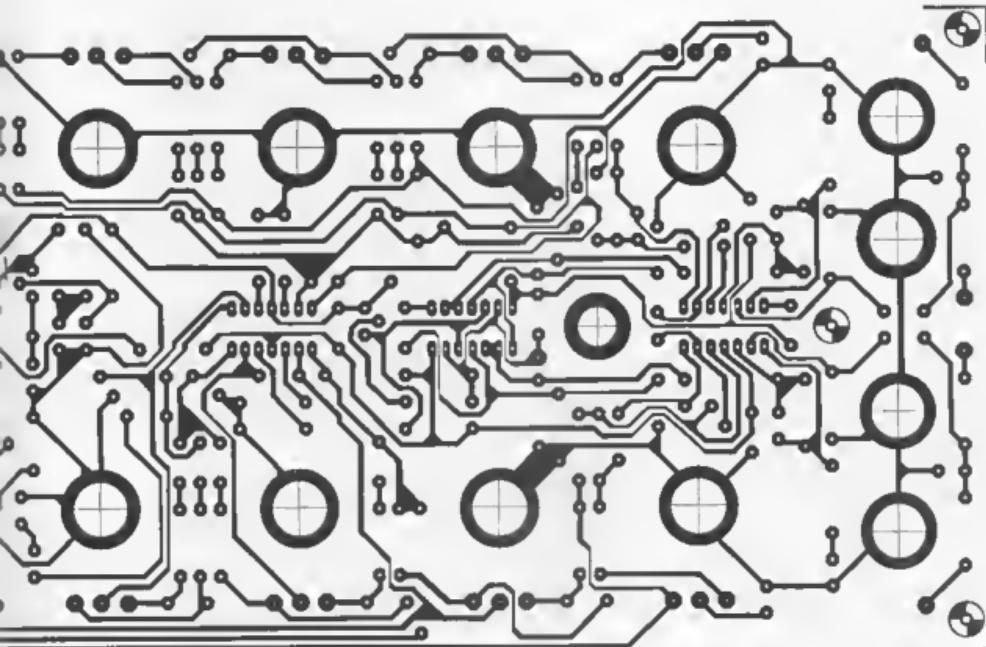


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that an input level of 7.5 mV is available to A1 and A3, irrespective of whether a high (less than 40 mV) or low (less than 10 mV) input signal is applied. The low noise opamp IC1 (A1, A3), amplifies this signal by a factor of 22, in order to achieve an excellent signal-to-noise ratio right from the start. The amplified signal (around 170 mV) is fed to either channel by means of CMOS switches ES1...ES4. S4 (channel change) is used for this purpose. A foot switch connected to the 8A4 socket bypasses S4 to allow remote control.

A close look at the circuit diagram in figure 1 shows that the input signal is switched around the different parts of the circuit by means of CMOS switches. The use of this method results in noiseless switching and good channel separation. The operating voltage of IC6 and IC7 is also reduced to about half ( $\pm 8$  V) their normal level, thereby reducing distortion. Potentiometers P1 and P7 set the input signal levels for channel I and II respectively. Opamp A2 in channel II is followed by the tone control circuit configured around A8. As readers will see this type of tone control network is practically standard and is common in all sorts of audio equipment. A4 in channel I is followed by a 5 band graphic equaliser giving  $\pm 15$  dB of cut and boost at 100 Hz, 300 Hz, 1 kHz, 3 kHz and 10 kHz. This is made up of a normal cut and boost tone circuit controlled by P8 and P9, and then by three band-pass filters around A6, A7 and A8.

Switches S2 and S3 control ES5 and

### 3



82014-3

When mounting onto metal front panel the use of plastic collar type sockets is recommended.

### Technical Specifications

frequency range	40 Hz ... 25 kHz
S/N ratio.	60 dB
noise factor:	0.1%
maximum output voltage:	4 V rms
nominal output voltage:	1 V rms
low input sensitivity:	10 mV
high input sensitivity:	40 mV
input impedance:	50 k
output impedance:	500 $\Omega$
tone control channel I:	
treble (10 kHz)	$\pm 10$ dB
middle (1 kHz)	$\pm 8$ dB
bass (100 Hz)	$\pm 10$ dB
tone control channel II:	
10 kHz	$\pm 10$ dB
3 kHz	$\pm 15$ dB
1 kHz	$\pm 15$ dB
300 Hz	$\pm 15$ dB
100 Hz	$\pm 12$ dB
reverb output voltage:	1 V rms ... 4 V rms
fuzz threshold:	1.5 V rms

### Parts list

#### Resistors:

R1, R39 = 56 k  
 R2, R40 = 15 k  
 R3, R6, R21, R22, R41, R49, R70, R76 = 220 k  
 R4, R24, R26, R28, R34, R37, R42, R68, R74,  
 R75, R79, R81 = 47 k  
 R5, R14, R31, R43, R66, R72 = 2 k  
 R6, R9, R27, R33, R44, R46, R69 = 33 k  
 R7, R45 = 12 k  
 R10, R47 = 3 k  
 R11, R48 = 1 k  
 R12, R13 = 4 k  
 R15, R16, R18, R19 = 5 k  
 R17, R20, R71 = 22 k  
 R23 = 27 k  
 R25, R32, R35, R38, R77, R80, R82 = 100 k  
 R29\* = 470  $\Omega$   
 R30 = 10  $\Omega$   
 R36, R50, R51 = 10 k  
 R52 = 680  $\Omega$   
 R53, R56, R57, R60, R61, R64, R65,  
 R67 = 150 k  
 R54, R55, R58, R59, R62, R63 = 8 k  
 R73 = 18 k  
 R78 = 10 M  
 R83 = 100  $\Omega$

P1, P7 = 47 k logarithmic

P2, P3, P4 = 47 k linear

P5, P13 = 10 k linear

P6 = 100 k log

PB = 22 k linear

P9, P10, P11, P12 = 100 k linear

P14 = 100 k preset

P15 = 22 k preset

#### Capacitors:

C1, C6, C33, C38, C56 = 33 n  
 C2, C34, C78 = 47 p  
 C3, C7, C35, C39, C43 = 100 p  
 C4, C8, C36, C40, C57, C59 = 2  $\mu$ 2/16 V  
 C5, C37 = 1  $\mu$ /18 V  
 C9, C10, C11, C20, C21, C22, C32, C55,  
 C58 = 10 n  
 C12, C14, C26, C29, C32, C54, C60, C62 = 47 n  
 C13, C48 = 1n5  
 C15, C53 = 22 n  
 C16, C79 = 15 n  
 C17, C28 = 220 n  
 C18 = 22 p  
 C19, C31, C44, C46, C61, C69 ... C77 = 100 n  
 C23 = 3 n3  
 C24\* = 10  $\mu$ /10 V tantalum  
 C25 = 100  $\mu$ /16 V  
 C27 = 1 n  
 C30 = 10  $\mu$ /16 V  
 C41, C42, C50, C52 = 4n7  
 C45 = 5n6

ES6 allowing either, or both channels to be 'patched' into the reverb loop. Once again the connection of foot switches to sockets Ba2 and Ba3 allows remote control of this facility. Opamp IC5 is the preamp for the reverb spring line. This is a standard ordinary amplifier which has been used in many other Elektor circuits. The gain of IC5 is set by R29 and C24. Obviously by changing these values IC5 can be altered to cater for the sensitivity of any particular spring line unit. With values as shown in figure 1 the output signal level from IC5 is about 4 V, making it ideal for the well-known 'Hammond' spring line, which has an impedance of approximately 8  $\Omega$ . The output level from the spring to A11, is set by P15, in order to provide the reverb circuit with unity gain. Calibration is quite easy, P15 should be set to give the same voltage at pin 8 of A11 as that of pin 3 of ES5. Bear in mind that without connecting a reverb spring line this procedure is not possible. The reverb intensity control (P5) mixes the 'flat' and 'contoured' signal.

The Fuzz circuit around the FET T2, is a little more complicated. T2 is made to operate at a drain source voltage level of around 500 mV, in other words, near to its pinching characteristic. As the FET is driven without feedback, the level of distortion at its output is dependent on the amplitude of the input signal. Increasing the input to channel I (P7) will provide a progressive increase in distortion, giving a tone reminiscent of valve amplifiers. Just as a matter of

C47, C49 = 27 n

C51 = 470 p

C63, C64 = 1000  $\mu$ /25 V

C65, C66 = 1  $\mu$ /25 V tantalum

C67, C68 = 4  $\mu$ /7/16 V tantalum

#### Semiconductors:

B1 = 840C1000 bridge rectifier (round version)

T1 = BC 547B

T2 = BF 256C, BF 245C

IC1 = XR4136, RC4136

IC2, IC3 = TL074, TL084

IC4 = LF 356, LF 356

IC5 = LM 386

IC6, IC7 = 4066

IC8 = 7808

IC9 = 7908

#### Miscellaneous:

S1 ... S4 = sp on/off switch (for single hole)

S5 = dp mains switch

Ba1 ... Ba3 = 1/4 in mono jack with switch

Tr1 = 2 x 12 V/200 mA mains transformer

La1 = mains LED indicator

F1 = 100 mA MT fuse with fuse holder

reverb spring line (Watford Electronics)

\* = see text



Figure 4. A suitable front panel layout.

interest, an input signal of 1.5 V would completely overdrive the FET and 'clipping' would result, just like any normal harmonic generator. As with the reverb circuit, P13 (Fuzz intensity) mixes the flat and distorted signals. The Fuzz 'loop' circuit has unity gain (set by P14), in other words, no change in volume when the Fuzz is by-passed.

Finally all the channel and effects 'loop' signals are mixed into the output stage (IC4) by way of the summing resistors R24, R33, R79, and the capacitors C29, C32, C62. The (master volume) P6 controls the overall output level.

The symmetrical power supply circuit uses two voltage regulators IC8 and IC9.

#### Setting up

This merely involves the setting of the two presets P14 and P15, which is easily done by using a multimeter set to 5 V AC. Calibration is not critical, an accuracy of  $\pm 5\%$  is sufficient.

A nominal signal is fed to one of the inputs of channel I (10 mV low, 40 mV high). If your signal generator is not provided with a meter, measure the voltage at pin 10 of A3 (IC1), and divide by 20. This will give a good indication of the input voltage level. Now set the wipers of all the equalisation potentiometers to their centre point. Rotate P7 until 1 V is measured at pin 1 of A9 (IC3). P15 is also set to give a reading of 1 V at pin 8 of A11 (IC2). The same procedure is repeated for channel II (do not forget to connect the reverb spring line), only this time P14 is turned up until 1 V is at pin 14 of A12 (IC3).

#### The printed circuit board

Almost all the electronic components and hardware are mounted on one single board, making construction simple and straightforward. The lack of normal wiring helps to keep noise and the possibility of mistakes down to a minimum. Even the wiring to the switches/sockets should present no problem as they only conduct DC voltages.

For the sake of economy no provision has been made for the mounting of the mains transformer and spring line onto the printed circuit board. Even so, readers will find no difficulties in connecting them up. Screened cable should be used for this purpose.

#### Construction

Standard (1/4 ins) mono jack sockets are used throughout mounted directly onto the front panel. Keep the connection wires as short as possible and use the plastic collar type of jack sockets, in order to avoid earth loops. A suitable front panel design is shown in figure 2. When using a metal front panel, care should be taken to ensure that none of the potentiometer spindles, toggle switches come into contact with it,

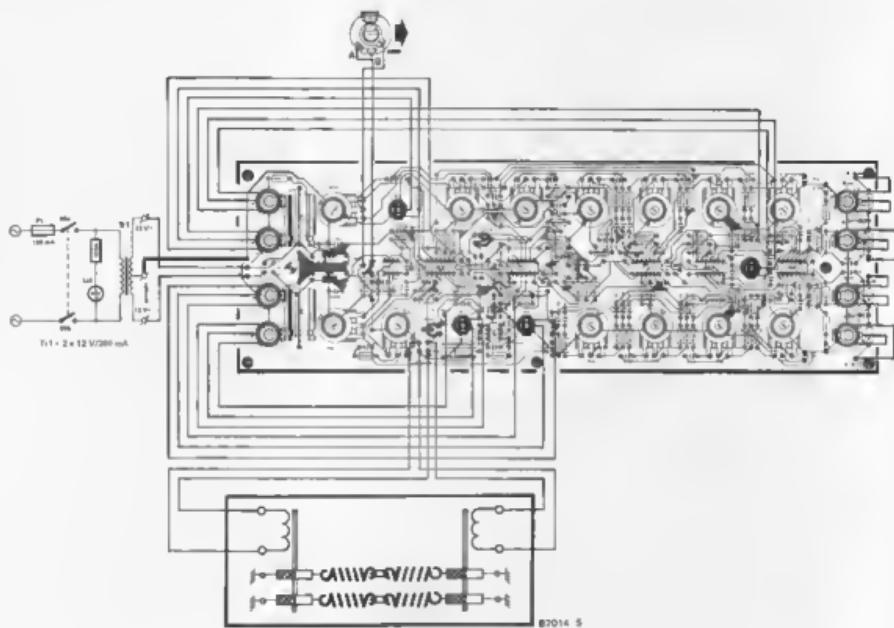
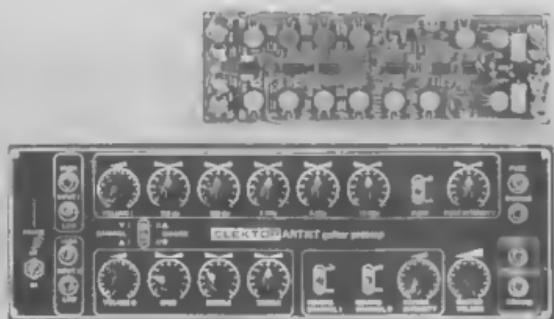


Figure 5. This clearly shows all connections to the p.c. board.

otherwise unnecessary noise is generated. This is specially important when considering the sockets, since the ground of the input has a different potential to the ground of the footswitch sockets. One good idea (as already advised) is to use plastic spindled potentiometers and insulated sockets. It is left to the reader to decide whether to leave the sockets on the board or not. Finally don't forget about the kind of power amplifier you are going to use. In principle, the Elektor Artist can be used with any. But please, bear in mind that it will not overcome all the shortcomings of some amplifier and speaker systems around.



As aeromodellers will know, it is necessary to match a particular propeller with any given engine. Each propeller has a specification, indicating the optimum efficiency relative to its 'speed' (rpm). Therefore a way of measuring its speed is essential. When an engine is being tuned it is also very useful to be able to check the rpm relative to any adjustment made. A mechanical method would prove costly and rather complicated to make. The only sure way to achieve a high standard with a relatively low cost is to use an electronic circuit. The speed of the propeller can be determined with the aid of opto-electronics. An analogue indication can be provided by means of a moving coil meter or, if digital is preferred, by using a digital display. Which method used will determine the cost.

### The circuit

The most straightforward part of the circuit is the power supply. For convenience and mobility a 9V battery is utilised. The power consumption is surprisingly low.

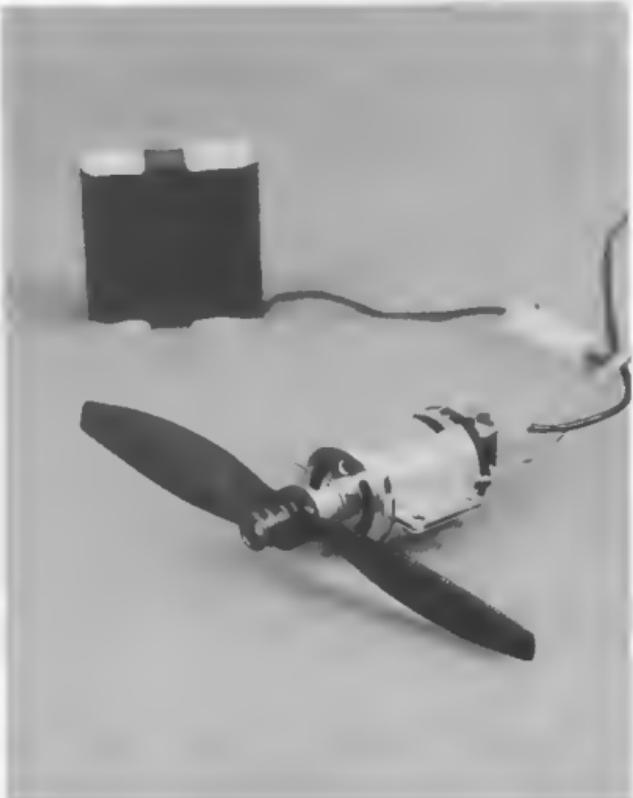
The signal from the photo diode or transistor D1, is amplified by opamp A1. With the turning 'prop' in front of the diode the amount of light falling on D1 will be fluctuating in direct proportion to the speed of the engine. It is advisable to place a dark-coloured 'prop' against a light background and a light 'prop' against a dark background. Diodes are included in the feedback loop of A1 to ensure that its gain will be logarithmic to compensate for changes in ambient light levels. R1 is also included to stabilise A1 when very little

# prop tachometer

a rev counter for model aeroplanes

Modellers tend to be rather slow in getting into electronics. This could stem from the fact that balsa wood and electronics are quite a few worlds apart, so that modellers may question their own skill with a soldering iron.

Expertise and reliability are certainly important factors where model aircraft are concerned, as any errors are inevitably costly. However, for certain applications, like the one described here, the simplicity of construction together with the help of a ready made printed circuit board, achieves a high reliability factor.



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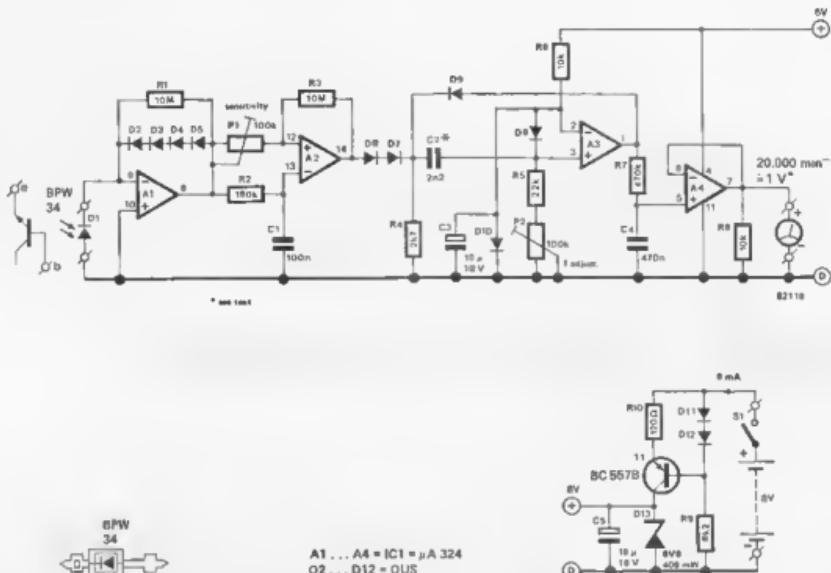


Figure 1. The circuit diagram for the tachometer. Note that a different output voltage range can be obtained by selecting a different value for C2; P2 is used for actual calibration.

light reaches the diode. If the circuit is only to be used outdoors, the diode can be replaced by a photo transistor connected as a diode (base and emitter only). This transistor is not as sensitive as the diode, but it will work reliably in normal daylight. It is strongly recommended that even when using the circuit indoors, readers should rely on daylight or a torch rather than on room lighting, as this could influence the accuracy of the circuit. The 100 Hz fluctuations tend to confuse the meter. Opamp A2 acts as a comparator and Schmitt trigger, converting the signals from A1 into square wave pulses for the frequency-to-voltage converter circuit around A3. The sensitivity of this stage is adjusted by P1, with the highest sensitivity at the lowest setting. In other words, the lower the switching threshold ( $P1 \rightarrow 0$ ), the higher the sensitivity, which implies that smaller signals will be detected by A2.

The frequency-to-voltage converter circuit may look complicated, but it is actually quite straightforward. Basically it is a monostable multivibrator (monoflop) triggered by the pulses from the Schmitt trigger A2. Each pulse is differentiated by C2, R5 and P2. The output

of opamp A3 will go 'high' when the pulse at its non-inverting input reaches the same value as that of its inverting input, thus causing a current flow through D9. Consequently capacitor C2 will discharge until the voltage at the non-inverting input drops below that of the inverting input. The output of A3 will then change state again until the next pulse arrives.

The remaining components in this part of the circuit ensure that the output pulse of A3 is proportional to its input pulse and the time it takes C2 to charge and discharge. The charge level of capacitor C4 will now be determined by the frequency of the pulses from the output of A3, since they are of fixed duration. In other words, this voltage level is proportional to the frequency of the changing light on the photo diode, (the input to the tachometer), and therefore the engine speed.

In the final stage opamp A4 acts as a buffer on the 10k load (R8). The output will then be within a DC range of 0 ... 1V. Photo 1 shows the characteristics of the tachometer. The horizontal axis indicates the number of revolutions with the vertical axis denoting the voltage. As



Photo 1. The output characteristic of the tachometer. The horizontal scale is 100 Hz (300 rpm) per division; the vertical is 200 mV/div.

can be seen, a good linear relationship exists between the two.

### Practical hints

Figure 2 shows the track layout for the printed circuit board. The battery can be attached to the board, if desired, by means of double-sided adhesive tape. It is strongly advised that the photo transistor (or diode) is mounted in some

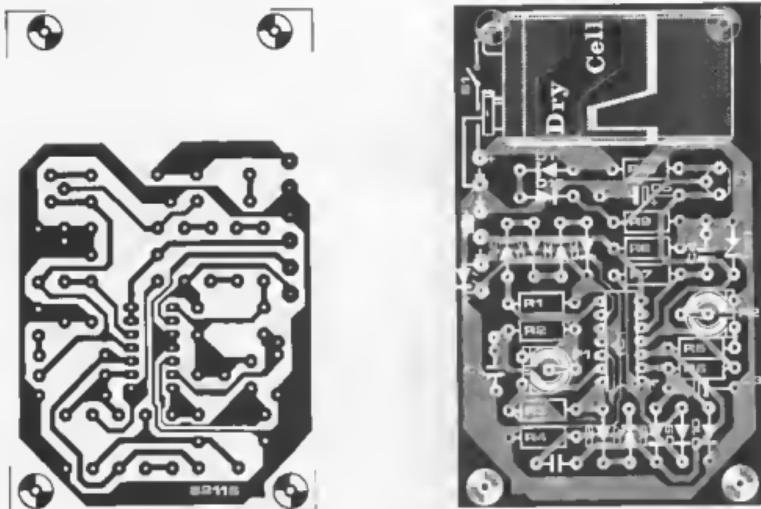


Figure 2. The track pattern and component overlay of the printed circuit board for the prop tachometer. The board has been designed to fit in a plastic case from Vero (202-21029J) or West Hyde (BOC 430). Since consumption is very low the battery will last quite a long while. In this case, it may be advisable to secure it with a piece of double-sided sticky tape.

#### Parts list

##### Resistors:

R1, R3 = 10 M

R2 = 180 k

R4 = 2k7

R5 = 22 k

R6, R8 = 10 k

R7 = 470 k

R9 = 8k2

R10 = 120 Ω

P1, P2 = 100 k presets

##### Capacitors:

C1 = 100 n

C2 = 2n2\*

C3, C6 = 10 μ/16 V

C4 = 470 n

\* see text

##### Semiconductors:

D1 = BPW 34 (Electrovalve) or phototransistor

D2, D12 = DUS

D13 = BZY 6V8 400 mW

T1 = BC 557B

IC1 = LM 324

##### Miscellaneous:

S1 = single pole on/off switch

9 V battery

form of protective 'handle' since it is known that fingers coming into contact with a prop turning at 15,000 rpm cause a sharp decrease in interest in all things concerned with aero modelling. Keep the connection wires between the diode and the circuit as short as possible.

#### Calibration

Setting up the circuit is very straightforward requiring the adjustment of only one potentiometer (P2). Connect a multimeter to the output, switch the circuit on and measure the offset voltage. Take careful note of this reading as it will be required later.

A normal fluorescent light tube can now be used as a calibration source. This is ideal because the light output varies in a 100 Hz rhythm (twice the mains frequency). This is equivalent to 6000 pulses per minute, or 3000 revs of a normal twin-blade propeller! Point the photo-diode at the lamp and adjust potentiometer P2 to give a reading on the multimeter of 150 mV DC plus the offset voltage, (the previously obtained reading). That's it, as far as calibration is concerned. The sensitivity is adjusted by means of P1, when measuring the revs

of a propeller. Obviously this setting will depend on the distance between the propeller and the diode or transistor, as well as on the contrast between propeller blades and background.

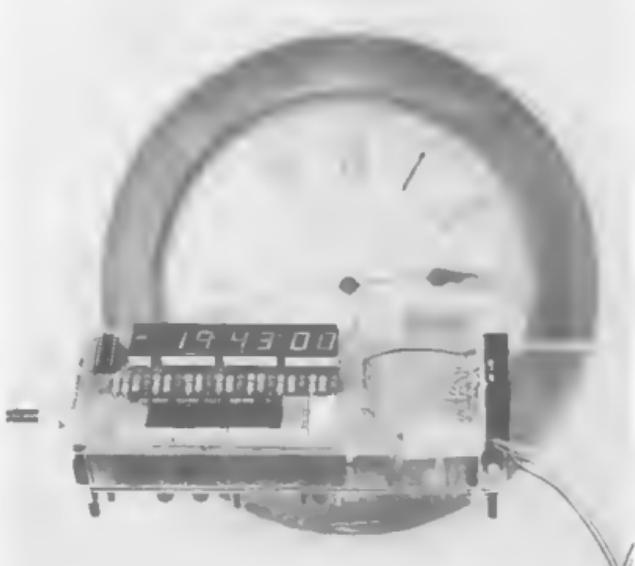
The choice of display is left to the constructors. A moving coil meter will be suitable and the offset voltage reading can often be eliminated by mechanically zeroing the meter. However, a standard multimeter or digital voltmeter will also do the trick, always remembering to subtract the offset voltage from the reading.

If desired, the voltage range of the output can be changed easily, since it is determined by the value of C2. As a rule of thumb, doubling the value of this capacitor will double the output voltage. The value given in the circuit diagram (2.2 nF) is a good choice: 20,000 r.p.m. corresponds to 1 V at the output. The maximum value for C2 is 6n8.

# 6502 housekeeper

## A programmable time-clock

With all the digital clocks and watches available today, it is surprising that time-switches are often such crude affairs. Given the relatively low cost of microprocessor chips, it seems 'logical' to do the job properly! This article describes a sophisticated time-clock, based on a 6502 microprocessor. It can be used to control a multitude of household appliances, such as cookers, burglar alarms and house lighting. Incidentally, since it must keep track of the time to do its job, it can also provide a digital display of time, day and date. In other words it is also a digital clock . . .



A 6502 microprocessor keeps track of the time and day of the week. It also calculates the date, even bearing leap years in mind, so that it will remain accurate until 'February 29th 2100'... (That is not a leap year, and most microprocessor-based 'perpetual calendars' go wrong at that point!).

Our electronic housekeeper is easily programmed. It provides four control outputs for switching purposes. Three of these are intended for 'daily needs' — 'on' and 'off' times are set on a 24-hours basis, and it is possible to select days of the week on which the sequence will not be executed. The times are accurate to within one minute. A fourth output is intended for a weekly cycle: ten 'on' and 'off' times are distributed over a seven-day period. The only restriction is that they must be set on a quarter-hourly basis.

The microprocessor checks the times entered; if a line seems to be switched off twice in succession, say, the 'housekeeper' will indicate this error immediately, during programming.

Obviously, this sort of thing requires an extensive program. A complete listing is included in this article, but we hope that enthusiasts will understand that we cannot explain it in detail... Describing the actual construction and operation of the time-clock takes up quite enough space as it is!

### The hardware

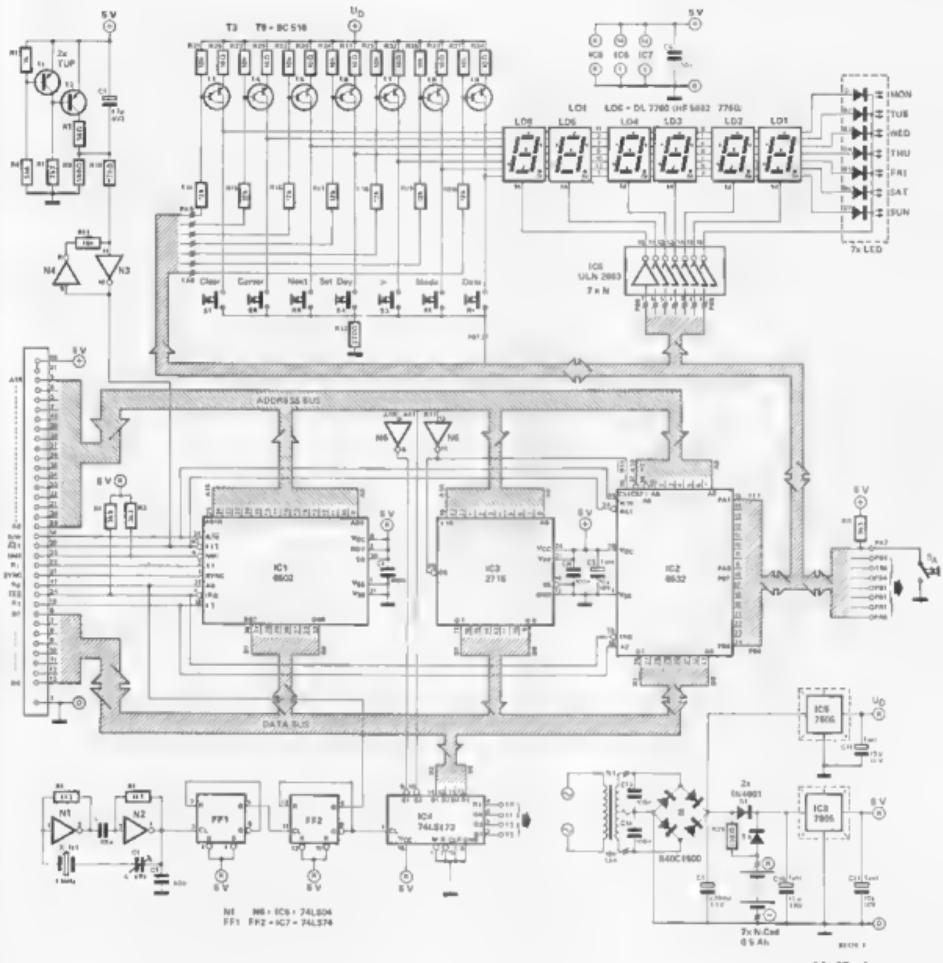
Figure 1 contains the complete circuit diagram of the digital time-clock. At the heart of the circuit there is a 6502 CPU (IC1). The program for the clock and the switch functions is stored in a 2716 EPROM (IC3). The third large IC is a 6532 (IC2), which provides 16 I/O lines to control the display, scan the keys and read in the time data. In addition, the IC includes a timer (which generates seconds pulses) and another 128 bytes of RAM to store temporary data and the switch time entries.

Apart from the 16 I/O lines to IC2, an additional four output lines are needed for the different switching times. These are provided by the four-bit latch, IC4.

The clock generator is shown at the lower left in the circuit diagram. The output from a 4 MHz crystal oscillator is divided by four to obtain the 1 MHz clock signal. This division is done by two flipflops, FF1 and FF2. Another alternative would have been to use a 1 MHz crystal in the first place, but the solution used here is a much cheaper way to obtain a 'clean' squarewave.

When the unit is switched on, a 'RES' signal is generated by the circuit around T1, T2, N3 and N4. Initially, T1 will not conduct but T2 will, effectively shorting capacitor C7 and ensuring that the output of N3 is at logic zero. T1 starts to conduct when the rising supply voltage reaches 4.5 V. As a result, T2 is turned off and C7 starts to charge,

1



**Figure 1.** The circuit diagram of the programmable time clock. The 6502 CPU is situated at the centre of the circuit. The displays and their control unit are shown at the top and the power supply is located in the lower right-hand corner.

Due to the C7/R9 time constant, the output of N3 stays low for some time after the supply voltage has attained its nominal value. The circuit around N3 and N4 is included to 'sharpen up' the edges of the reset pulse. In passing, we can note that a reset pulse is also produced if the supply voltage briefly drops below the 4.5 V level for any reason, but this will be discussed later.

on.  
One side of the student's notebook

LEDs is connected to the I/O lines by means of the buffer/inverters in IC5, and the other is linked to the darlington transistors, T3...T9. The latter see to it that a constant current flows through the displays and the LEDs. Two 5 V stabilizers, IC8 and IC9 pro-

Two 5 V steppers, IC6 and IC5, produce the supply voltage. They both provide 5 V, IC9 feeding the LEDs and displays and IC8 looking after the rest of the circuit. This arrangement makes

(NICAD) battery supply. The batteries are placed at the input of IC8. During normal mains operation, a 'topping-up' current flows continuously through the batteries by way of resistor R35. In the event of a power failure, the batteries will feed the main circuit via D9 and IC8. At the same time, a very low current will pass through the displays (by way of R35 and IC9). This system reduces the current consumption

batteries used here will be able to stand in for about one and half hours.

The charge current flowing through the batteries is determined by the value of R35. This in turn depends on the transformer voltage and may be calculated as follows:

$$R35 = \frac{U_{C9} - 10}{20 \cdot 10^{-3}} = 50 U_{C9} - 500 \Omega$$

During prolonged power cuts the batteries may be discharged to such an extent that the stabilised supply voltage drops below 4.5 V. In that case, the reset circuit will introduce a reset to prevent errors in the program execution and failure of the display multiplexing unit (which might cause one of the displays to burn out!). The reset will also cause the programmed switching times to be lost. Fortunately, a power failure will rarely last longer than 90 minutes!

Instead of NICADs, two ordinary 4.5 V batteries may be connected in series, in which case R35 is omitted. They will have to be replaced after a year or two, of course. Some readers may even consider this emergency supply totally superfluous, in which case the batteries, R35 and D9 may be left out altogether and DB may be replaced by a wire link.

The address decoding system does not need to be complete and a simple circuit (using only two inverters) will suffice, because the memory range consists of only three blocks (IC2...IC4). The processor can deal with a total of 64K memory, but what happens here is that the same 4K memory block is repeated throughout the range. The three blocks are decoded by address lines A10 and A11:

A11      A10

0	0	IC2
0	1	IC4
1	0	IC3
1	1	

Memory is mapped as follows:

*000	*400	*800
· IC2	· IC4	· IC3
·	·	·
*3FF	*7FF	*FFF

(\* = don't care)

The chosen structure is by no means coincidental. The EPROM is at the top end of memory, because that is where the NMI, RESET and IRO vectors have to be fetched. IC2, the 'RIOT' (this stands for RAM, I/O, TIMER - a well-organised IC, despite its name), is situated at the other end of the range for two reasons:

- Using the 6502 µP, 'zero page instructions (addresses 0000...00FF) are only 2 bytes long. If similar instructions are required on any other page they will consist of three bytes. This is a highly effective way in which to economise on memory space.
- Page 1 (0100...01FF) must contain

```

HEXDUMP: 0800..0FFF
 0 1 2 3 4 5 6 7 8 9 A B C D E F
0800: D8 A9 FF AA E8 95 00 E0 3D 00 F9 A9 88 E8 95 00
0810: E0 47 D0 F9 00 85 0F 85 21 B0 00 F9 A9 88 E8 95 00
0820: E8 E0 3E D0 F9 E6 4C E6 61 A9 7F 85 00 81 85 83 85
0830: 60 AA 9A 58 00 EA EA 20 4H 09 C9 FF D0 F9 A9 87
0840: A2 00 A0 00 24 87 50 11 A2 00 E8 CB 20 8C 0B C0
0850: 28 F0 5C A5 80 10 F4 30 F1 20 8C 0B E8 E0 28 D0
0860: E3 A5 5F C9 59 D0 3F A2 96 20 8C 0B CA DO FA A2
0870: 07 A0 06 20 9F 09 A2 05 B5 4F D5 55 D0 17 CA 10
0880: F7 A2 05 B5 55 95 4F 95 49 CA 10 F7 20 32 09 A2
0890: 08 86 61 A2 DB 86 9F 85 48 85 60 30 A1 A2 05 B5
08A0: 55 95 4F CA 10 F9 A2 FF 86 60 20 32 09 30 8F E0
08B0: 0A 90 F3 E0 1E 90 04 A9 80 00 02 A9 00 85 63 A4
08C0: 5F C0 20 9B 2B 30 C5 A5 63 10 02 E6 5D 65 5E C0
08D0: 2B F0 38 CO 35 F0 32 CO 41 F0 3C C0 44 F0 42 C0
08E0: 49 F0 45 C0 57 F0 46 CO 58 F0 20 15 55 DA 94 55
08F0: A2 96 20 88 02 CA DO FA 1A 98 F8 69 01 08 05 5F
0900: 42 3E 08 A5 63 30 E9 10 9D 55 45 46 5B 97 A9
0910: 08 85 5D E6 5E 5D DO D9 19 55 4A 4A 95 55 E8 5E D0
0920: CF 15 55 4A 4A 4A 10 F1 15 55 4A 10 E8 15 55 4C
0930: 1B 09 A2 OA A9 00 95 55 CA 10 F9 66 85 58 84 5C
0940: 46 62 90 12 A2 Q2 B5 4B EO 02 D0 03 20 89 09 95
0950: 67 CA 10 F2 30 12 A5 4B 20 89 09 85 69 15 A4 20
0960: 89 09 85 68 A5 4E 85 67 A6 4C A9 7F 38 DA CA 00
0970: FB 85 66 A5 60 FO EA E6 11 E6 11 10 04 A9 FF 85
0980: 62 2B 13 OB A6 5B A4 SC 60 A8 F0 06 C9 0F B0 02
0990: 09 F0 60 A0 01 20 08 01 49 60 D0 60 99 48 00 20
09A0: 08 04 49 60 D8 64 99 49 00 20 08 01 49 60 99 48 00 20
09B0: 99 4A 00 20 08 02 0A 20 08 02 OA C9 08 02 D0 A9 01 99
09C0: 4C 0B 89 4B C9 29 3B 41 C9 31 30 11 6A 90 26
09D0: B9 40 00 C9 08 10 02 49 FF 6A 80 1A 90 22 89 4D 20
09E0: 00 C9 02 D0 25 B9 4E 00 29 13 F0 04 C9 12 D0 06
09F0: B9 4B 00 6A BA 14 A9 01 99 4B 00 20 08 0A C9 13
0A00: D0 A9 01 99 4D 00 20 08 0A 60 18 85 4B 48 F8 69
0A10: 01 D8 95 4B E8 60 48 98 4B 8A 48 A9 00 85 81 A5
0A20: 82 85 64 C6 61 F0 08 A5 01 A9 79 85 9F DO 1B A9
0A30: 82 85 9E A5 10 F0 07 A5 48 D0 03 20 58 04 A2 00
0A40: 20 93 09 20 29 OA A9 09 85 61 A5 64 85 82 A9 7F
0A50: 85 81 68 AA 68 A8 68 40 85 01 A2 02 A9 09 A8 8A
0A60: 0A 0A 0A 05 0E B1 0E 0A A4 CO 0A 88 DF FC 90
0A70: 08 AF 2B 05 01 85 01 BO F1 C8 C8 A5 4A D1 0E F0
0A80: 04 B0 0A 90 13 A5 49 C8 D1 0E 90 0C 88 C8 A9 01
0A90: 45 01 85 01 C0 09 00 E2 06 01 CA 10 BF 66 01 E8
0A90: E0 14 F0 25 20 D5 0A 98 C5 4C 90 F3 D0 1B 85 2A
0AB0: 4A 4C 5C 4A FO 0W 90 0E BO 0F B5 2A 29 03 A8 A5
0AC0: 49 D9 F3 FO 09 03 4C 9F 0A 8A 29 01 OA 0A 04 0A 05
0ADO: 01 BD 00 04 60 8A 4B 4A AA B5 3E 90 08 4A 4A 4A
0AE0: 4A 48 68 AA 60 29 0F 10 F8 A2 00 8A 09 60 85 82
0AF0: A8 C9 09 00 D2 E8 8A 4A A8 99 09 B9 48 4B 4A 4A
0B00: 4A 1A 10 03 B9 48 00 29 0F 09 30 85 82 E8 EO 0E
0B10: DO D9 60 A9 40 85 1B A2 04 A9 02 85 IC B5 65 C6
0B20: 1C FO 27 30 29 4A 1A 4A 4A A8 89 DB OF A4 1B 84
0B30: 82 85 30 20 86 80 A5 21 C9 01 FO 07 25 1B FO 03
0B40: 20 86 08 88 84 80 16 1B 10 D3 29 0F 10 DO CA F0
0B50: 09 EO 01 DO C4 B5 65 4C 2D 0B A5 21 FO 04 C9 01
0B60: DO 03 20 86 0B A9 00 85 82 A9 BF 85 80 A5 82 D0
0B70: 09 A5 08 09 80 6A 85 80 B0 F3 A5 80 09 80 85 62
0B80: A2 FF 86 80 AA 60 A4 88 00 F7 60 20 3C 09 C9
0B90: FD 00 F8 20 13 OB A2 7F 9A 20 4H 0E 20 13 OB E8
0BA0: 00 FA 20 13 OB E8 FO FA 20 13 OB E8 FO 2F C9 EF
0B80: F0 11 C9 BF FO 13 C9 DF FO 06 C9 FD FO 47 36 E2
0BC0: IC AF OC 20 54 0E IC 9C OB A2 FF 86 69 86 68 A9
0B00: 2A 05 04 FO 1D 49 02 C5 DO 00 82 66 A9 0A C5
0BEO: OB FO 09 20 E6 0B E6 0B 10 F1 20 48 0E 4C
0BF0: 9C 0B 86 66 20 E6 0E E6 0B A9 14 C5 OB 00 F5 20

```

RAM for the 'stack'. This requirement is met by not connecting address lines A8 and A9 to IC2 (RIOT will therefore occupy pages 0...3). This means that the 128 bytes of RAM in IC2 are used for two different purposes. The lower section belongs to page zero (0000...0069) for storing data (intermediate results and switching times), whereas the rest acts as the stack in page 1 (016A...017F).

Finally, the address range between RIOT and EPROM is used for the latch (IC4).

## Construction and calibration

Figures 2 and 3 show the printed circuit boards for the digital time-clock. One board contains the displays, LEDs and keys and the other accommodates the processor, with its associated components and the power supply. The boards are designed to be mounted one on top of the other, with the copper sides facing each other. Be careful when wiring the boards and inserting them into a case. Some mounting holes are drilled through wide copper tracks. Use

```

OC00: 44 0E 4C 9C 0B 20 44 0E A9 02 C5 0B F0 25 A5 69
OC10: 85 1A A5 68 85 1B C6 0B C6 0B 7C 0E A5 69 C5
OC20: 1A F0 04 B0 5F 90 08 A5 68 C5 1B F0 02 B0 55 E6
OC30: 08 E6 0B A9 02 C5 0A D0 06 A9 08 C5 0D F0 06 20
OC40: 54 0E 4C 08 06 20 48 0E A5 69 85 5B A5 68 85 5C
OC50: 24 D5 0A C0 08 F0 28 84 1A E8 86 0B 20 AF 0E 98
OC60: C5 1A 90 20 F0 02 B0 11 EA A5 69 C5 5B 9D 15 F0
OC70: 02 B0 06 A5 68 C5 5C 90 0B A5 DB C9 13 D0 C9 C6
OC80: 1D 4C 37 08 A9 CD 85 69 A9 DA 85 68 A9 DF 85 67
OC90: A9 FF 85 66 85 0D 20 13 0B C6 0D D0 F9 A9 2A C5
OCAC: OA F0 06 20 50 0E 4C 9C DB 20 68 0E 4C 9C 0B A6
OCBO: 69 E8 D0 04 86 69 86 68 A9 89 85 21 A9 2A C5 0A
OCCO: FO 3A 99 02 C5 09 F0 2A 40 21 A9 01 C5 21 D0 04
OCDO: A9 03 85 21 A9 02 C5 21 F0 1B A9 40 C5 21 F0 1C
OCEO: 4A C5 21 F0 30 4A C5 21 F0 25 4C A5 21 F0 23 4C
OCFO: 83 03 4C 95 0D A9 08 85 21 4C 9C 08 20 4F 0F A5
OD00: 69 18 66 10 C9 24 90 02 A9 00 85 69 4C FC 0C 4C
O010: 3C 0D 4C 65 0D 20 4D DF E6 69 A9 20 25 69 F0 0C
O020: A5 69 C9 24 0D EF A9 20 85 69 10 E9 A5 69 29 0F
OD30: C9 0A D0 E1 A9 20 25 69 85 69 10 D9 A9 2A C5 0A
OD40: F0 13 20 4D OF A5 68 18 69 10 C9 60 9D 02 A9 00
OD50: 85 68 4C 42 00 A9 18 85 21 20 40 0F 18 A5 68 F8
OD60: 69 15 D8 C9 60 D0 02 A9 08 85 68 4C 59 0D 20 4D
OD70: 09 E6 68 A5 62 29 OF C9 0A D0 F3 A9 F0 25 68 85
OD80: 68 10 EB 20 4D OF A2 2A E4 OA 00 0A A2 FF 86 0A
OD90: 28 48 0E 4C 83 OD A9 00 85 21 20 97 OF E8 D0 FA
ODAQ: 29 97 OF E8 FO 2A 97 OF E8 FO F4 C9 DF FO 49
OD80: C9 EF FO 4F C9 FB DO E8 A9 2A C5 0A FO 4B A9 80
ODCO: 85 OC A9 FF 85 66 46 OC 20 B6 OF E8 DO FA 20 B6
ODDO: OF E8 FO FA 20 B6 OF E8 F0 F4 C9 DF FD 1B C9 EF
ODEO: F0 21 C9 F0 FO 0A C9 F7 DO EA 05 OC 45 66 85 66
ODFO: A9 01 C5 OC D0 DO 4C 9A 0D 20 E6 OF E8 A9 80 85 21
OE00: 4C C8 0C 28 E8 0C C8 C3 09 A0 01 09 F0 04 CA
OE10: 2B D8 0A B9 E9 OF 85 66 49 FF 85 0C 20 B6 OF E8
OE20: DO FA 20 B6 OF E8 FO FA 20 B6 OF E8 FO F4 C9 FB
OE30: F0 07 C9 F7 D0 EC 4C 96 0D 46 OC A5 OC FO CA 38
OE40: 66 66 30 D8 A9 FF 85 0A E6 QA A9 D3 C5 0A FO 18
OE50: A9 00 85 0B A9 2A C5 0A FO 16 E6 OF E8 OB A9 0A
OE60: C5 0B FO F4 20 7C 0E 60 A9 2A 85 0A A9 FF 85 0B
OE70: E6 OB A9 14 C5 OB FO CC 20 AF 0E 60 A9 0B A8 85
OE80: 10 A5 0A OA OA OA OA AA 05 OB 85 IC B1 IC 85 69
OE90: E6 1C B1 1C 85 68 1B C5 0B A8 64 60 90 0B A9 0B
OEAO: 05 1C 85 67 86 1C B1 IC 85 66 60 A9 0A 10 F1 A5
OEBO: OB AB 52 2A AB C9 FO 23 29 FC 94 4A 85 69 B5 2A
OECD: 29 03 AB B9 F3 OF 85 68 8A 4A 90 16 A9 04 09 30
ODEO: 85 67 EB 20 D5 OA B9 EA OF 85 66 60 88 8A 69 84 68
OEEO: 3C E8 A9 0B 10 AE A5 0A C9 2A FA 18 OA 0A OA OA
OEFO: 85 1C A0 00 A5 66 91 1C A4 OB A5 69 91 IC CB A5
OF00: 68 91 IC 60 A0 00 A5 OB AA 55 69 0A 0A 95 2A A5
OF10: 68 FO 09 C8 C9 15 FD 06 C8 C9 3D F0 D1 C8 98 15
OF20: 2A 55 2A A0 00 A9 7F C8 38 6A C5 66 00 FO F9 8A 4A
OF30: AA B5 3E 90 GE 29 OF 95 3E 98 0A 04 DA DA 15 3E
OF40: 95 3E 60 29 FO 95 3E 98 15 3E 98 60 8D 20 81 0F
OF50: E8 00 FA 20 81 OF E8 FO FA 20 81 0E FO F4 C9
OF60: D8 FO 09 C9 EP OF C9 FG D8 6B 2A BE 88 9A
OF70: 20 E6 0E 4C 0C 0A A9 08 85 21 BA S8 E8 9A 4C 03
OF80: 08 A5 21 85 1A E6 00 E6 0D 10 D9 A9 00 85 21 20
OF90: 13 Q8 A4 IA 84 21 6D E6 D0 A9 T9 25 OD DD 12 A5
OFAD: 66 49 FF 85 66 20 13 OB A5 66 49 FF 85 66 A5 62
OFBD: 60 20 13 OB D0 FB E6 DD B6 OD 10 A5 66 85 1A
OFC0: A5 OC 45 66 85 66 20 13 OB A5 1A 85 66 A5 62 6D
OFDD: 20 13 OB D0 FB 18 90 FO FF FF FO 40 79 24 30 19
OFE0: 12 02 78 00 10 23 7B 06 2P FF FF BF OF EF F7 FB
OFF0: FD FE FF 0C 15 30 45 FF FF FF D5 OF 00 08 16 OA

```

insulated spacers and screws here, as otherwise something may well go up in smoke!

The 'day' LEDs can best be flat rectangular types (such as HP 5082-4670). The days of the week can be indicated on the LEDs by means of transfer lettering. Different shaped LEDs may also be used and the days may be printed next to each on the front panel. A third option is to mount an LED array in a DIL package (a set of 10 LEDs, such as the MV 57164, for example) and carefully remove three of

them with a saw.

The two regulator ICs must be properly cooled. The back of the metal case can act as the heat sink if the regulators are mounted directly onto it, but mica insulation and washers must be used. The pins of the regulator ICs should be soldered onto the board, by the way, not wired. It is quite feasible to separate the supply section from the rest of the board, if desired, and mount it elsewhere in the case.

The boards are connected so that both sets of P80...P86, PA0...PA6 and

PA7 pins are opposite each other. The connection points can then be linked with short lengths of wire. Then connect the three power supply connections on either board.

Once construction is complete you could insert all the ICs, connect the transformer to the mains and check whether everything is working satisfactorily. If something is wrong, it would be quite a problem to trace the error with a logic analyser. But there is another method, and a few hints on how to test the hardware using an oscilloscope or a multimeter can make all the difference.

Don't connect anything up for the moment, except for the stabilisers IC8 and IC9. Don't insert the other ICs into their sockets yet! The same applies to the batteries. Now check whether the output voltage of the two stabilisers is 5 V. Switch off the supply and insert IC6 and IC7. Switch on the power again and see whether there is a symmetrical 1 MHz squarewave at pin 8 of IC7. Readers who do not own an oscilloscope may use a multimeter instead and the auxiliary circuit in figure 4a. If the oscillator is working properly, the meter will indicate about 0 V. (A reasonably good frequency counter is needed to check the frequency; calibrate the oscillator with C2.)

Now find out whether RES (pins 9 and 10 of IC6) is logic 1. If so, the code 'AA' is applied to the data bus by means of several wires and resistors, as shown in figure 4b. The indicated numbers refer to the connector pin numbers between IC1 and IC3 on the board.

Time to insert the 6502 (IC1) in its socket (turn the power off first!). After power up, a symmetrical squarewave with a frequency of 250 kHz should appear at A0 (connector pin 29), 125 kHz at A1, 62.5 kHz at A2, and so on down to 7.6 Hz at A15. R/W (connector pin 14) must remain high. If one of the above conditions is not fulfilled, first check whether AA is in fact being applied to the data bus. Again, this measurement does not require an oscilloscope and can be carried out by means of the auxiliary circuit in figure 4c. The circuit is connected to all consecutive pairs of address lines in turn: A15 and A14, A14 and A13, A13 and A12...A1 and A0. Each time the meter should read either 0 V or 5 V. Any intermediate value indicates a fault. It is best to check whether there is a 7 Hz squarewave at A15 first by connecting the meter to it. The pointer will 'flutter' at this very low frequency (provided you are using a moving coil meter). Then check all the address line pairs with the auxiliary circuit.

The 'AA code' is now disconnected from the data bus. Remember, no soldering while IC1 is on the board! It will have to be removed from its socket each time. The next step is to mount the EPROM, IC3 (with the power off, of course!). Before switching on the power

2

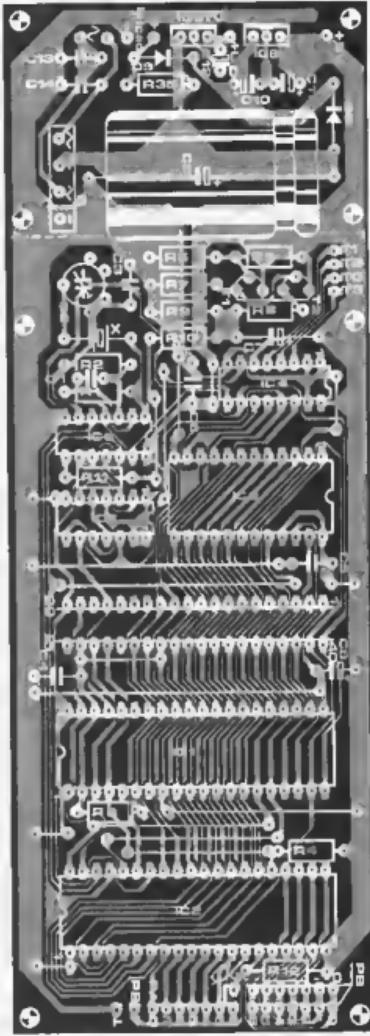
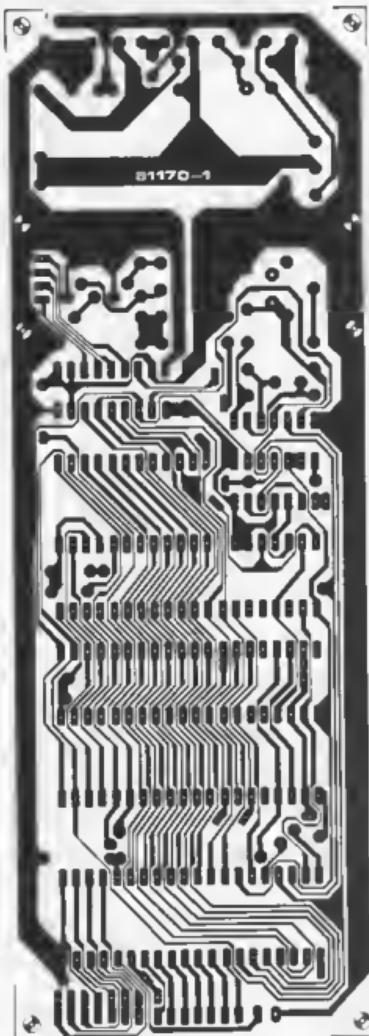


Figure 2. The main printed circuit board. This accommodates the entire microprocessor unit. The power supply section may be separated, if necessary.

#### Parts list

##### Resistors:

R1, R2, R7 = 2k2

R3, R4, R12 = 3k3

R5 = 1 k

R6 = 5k6

R8 = 56 Ω

R9 = 560 Ω

R10 = 470 Ω

R11 = 15 k

R13 = 220 Ω

R14 ... R20 = 12 k

R21 ... R27 = 10 k

R28 ... R34 = 10 Ω

R35 = 120 Ω

##### Capacitors:

C1 = 10 n (cer.)

C2 = 4 ... 40 p trimmer

C3 = 150 p

C4, C5, C6, C13, C14 = 100 n

C7 = 47 μ/6.3 V

C8, C11, C12 = 10 μ/10 V (tent.)

C9 = 2200 μ/25 V

C10 = 10 μ/25 V (tent.)

##### Semiconductors:

T1, T2 = TUP

T3 ... T9 = BC516

IC1 = 6502

IC2 = 6532

IC3 = 2716

IC4 = 74LS173

IC5 = ULN2003

IC6 = 74LS04

IC7 = 74LS74

IC8, IC9 = 7805

D1 ... D7 = LED red

see text

D8, D9 = 1N4001

B = B40C1500 bridge rectifier

L1 ... L6 = DL 7760

(HP 5082-7760)

##### Miscellaneous:

Tr = 10 V/1.5 A mains transformer

S1 ... S7 = digitast

X = 4 MHz crystal

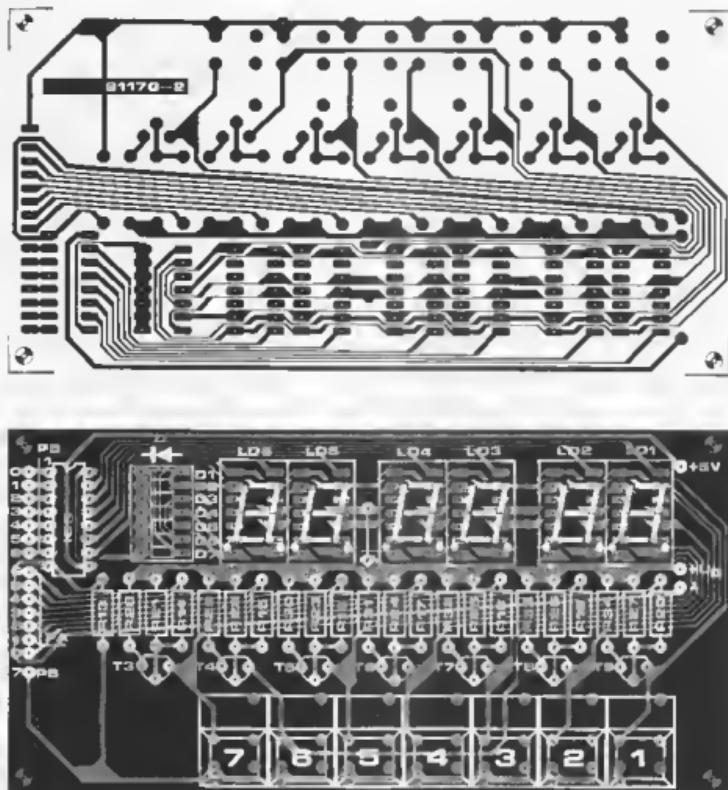


Figure 3. The display board contains the displays, LEDs, control electronics and pushbutton keys.

supply again, link pin 26 of the connector (NMI) to pin 36 (A7). After power up, the address bus should read:

A15	A14	A13	A12	A11	A10	A9	A8
0	0	0	0	1	1	1	1
A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	1	-	-	-	-

(A3...A0 are not stable)

Furthermore, pin 20 of IC3 should be constantly low. If something is wrong, either the EPROM was not correctly programmed or N5 is not inverting the signal.

If everything is O.K. so far, pull out the mains plug for the last time, remove the connection between NMI and A7 and insert the remaining ICs. The clock should start to count from 00 00 01 as soon as the circuit is switched on.

Calibrating the crystal oscillator accurately is not an easy job. As mentioned earlier, the oscillator can be adjusted with C2, with a quality frequency meter connected to pin 8 of IC7. However, as few readers will be fortunate enough to

own a really accurate frequency meter, here is an alternative method. It can be just as accurate, but it is rather more time-consuming...

First set the trimmer capacitor C2 in its centre position. Switch on a radio and wait for the time signal on the hour (1100, 1200, etc.). Synchronise the clock on the sixth 'pip' of the radio time signal and press the start button. Let the clock run 'on its own steam' for several hours and then compare it to 'real time' again. Check whether the oscillator is 'fast' or 'slow' and readjust it with C2, if necessary. By repeating this procedure several times (over a period of a few days, if necessary) readers will be absolutely sure the oscillator is accurately calibrated.

#### Programming the timer

A pushbutton switch (S4) is connected between the input and ground to start the time entry routine. Operation is as follows. After power up, the clock starts to count from 00 00 01. The clock is

stopped by depressing S4. The week/day LED then flashes. The desired day of the week may be selected with the > pushbutton (S3). Then the CURSOR key is operated (S6) and the tens/hour display starts to flash. The hours may be set by depressing > several times. The hours, minutes and seconds are all dealt with in the same manner. Once the 'second' units have been entered and the CURSOR key is operated again, the date will appear on the display. The same procedure is followed to enter the correct date, starting with the day and ending with the year (from left to right, in other words). Take care not to program an impossible date, as the clock might feel inclined to misbehave. After the year entry press the CURSOR key again. The time will then reappear on the display but no LEDs will flash. Now press the MODE key (S2) and the clock will start one second later. Readjust the time or date setting with the S4 key, if necessary. By the way, S4 doesn't have any effect unless the clock is 'ticking'!

4

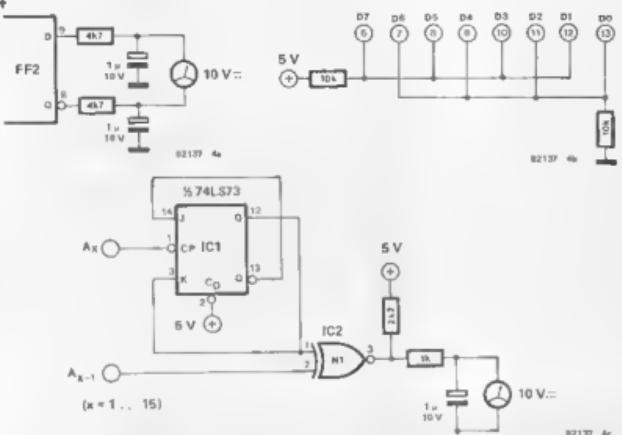


Figure 4. The auxiliary circuits for testing the digital time clock. They are only required if an oscilloscope is not available.

5

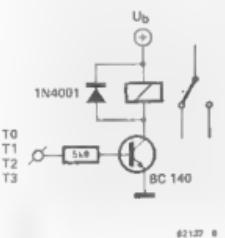


Figure 5. This tiny 'interface' enables outputs T0...T3 to switch mains-powered equipment on and off.

Nothing happens if it is operated during the switch time entry routine, which is described below.

The four control outputs may be connected to any device that needs to be switched on or off at a specific time by means of a relay or a triac circuit. Outputs T0...T2 can each program four switch times within 24 hours. In addition, the day of the week may be entered on which these switch times are to be processed. Every day at 00.00 hours the outputs T0...T2 are automatically reset. The minimum switching interval (between 'on' and 'off') is one minute.

The fourth output, T3, can be programmed for a weekly cycle. It provides 10 'on' and 10 'off' times that can be set at fifteen-minute intervals. This line is automatically reset at the beginning of every week (at 00.00 hours on Monday morning).

The switch functions are as follows:

- S1, the DATE key, displays the date.
- S2, The MODE key, selects between the time display and the switch time entry.
- S3, the > key, increments the value on display that is indicated by a flashing cursor.
- S4, the SET DAY key, serves to program the days of the week.
- S5, the NEXT key, shows the next switching time on the display.
- S6, the CURSOR key, moves the cursor from left to right across the display (but not the right-hand digit); that indicates whether an 'on' and 'off' time is involved). The display selected by the cursor flashes to indicate that it may be altered, if necessary, with the > key.
- S7, the CLEAR key, deletes some or all of the switching times on a particular line (starting with the time currently on display).

As mentioned above, the right-hand display indicates whether the switching time shown refers to 'on' or 'off'. 'On' is represented by a '1' and 'off' by a '0'. Its neighbour shows the line number (0, 1, 2 or 3). A program example is included in this article to illustrate how the various keys work, and to give an idea of the facilities.

A return to the normal time display routine causes T0...T3 to be modified according to the entered switching times. This occurs exactly one second after every minute period. During programming of the switching times, the outputs remain unchanged.

One final point. If an 'off' time is programmed and this turns out to precede the 'on' entry, depressing the MODE key will cause an ERROR message to appear on the display for a few seconds, followed by the first time that is programmed for the line where the error occurs. No return can be made to the time display. First the error must be corrected, after which the MODE key is operated to switch the processor back to time display.

### Switching mains-powered equipment

Readers who wish to switch mains-powered equipment 'on' and 'off' with the aid of the time switch require a small interface for each of the four switch outputs. Figure 5 provides a simple circuit for this purpose. The switch output controls a transistor by way of a resistor. The relay can then switch a device on and off. How much power may be switched depends on the type of relay. For the transistor shown, the relay current should not exceed 100 mA. If 12 V relays are to be used they may be connected directly to the time clock's power supply (across C9). This method ensures that the circuit is electrically isolated from the mains voltage. A solid state relay is of course equally suitable.



## Program example

Switching times to be programmed:

line T0: switch on at 08.30 on Monday and Friday  
switch off at 09.02

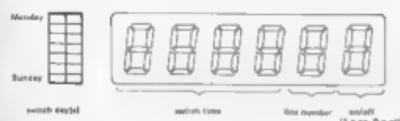
line T1: constantly '0'

line T2: constantly '0'

line T3: switch on at 20.00 on Sunday  
switch off at 08.00 on Tuesday  
switch on at 10.00 on Wednesday  
switch off at 00.45 on Thursday

	indicates a day LED is ON/HI
	indicates a day LED is HI
	indicates a day LED is Flashing
	indicates a display is Off/Flickering
	indicates a display is HI

display shorthand



> (3x) 083001 minutes time belonging to first 'on' time we programmed

NEXT 00    the next 'off' time is selected

CURSOR (3x) 000000 the hours may be changed, the day LEDs do not have to be changed, because this time is programmed per day

key    display    comments

MODE 0    change to switch time entry

> (4x) 090000 hours we programmed

CURSOR 000000 days flash to indicate they may be programmed

CURSOR (3x) 090000 cursor shifts two places to the right

> 000000 Monday LED is flashing

> (2x) 090200 left time of T0 is now stored

SET DAY 000000 Monday is stored

NEXT 01 select flash switch time

> (3x) 000000 Friday LED is flashing

CLEAR 000000 the last two switch times of T0 are erased, because they are not needed. The display reports back with the first 'on' time 01

SET DAY 000000 Friday is stored too

CLEAR 21 T1 is not used yet, may therefore be erased. T2 appears

CURSOR (2x) 000000 More units are flashing to indicate they may be changed

CLEAR 31 T2 is stored and T3 appears

> (8x) 080000 More belonging to time switch-on time is programmed

CURSOR 000031 cursor flash to indicate the first 'on' time of T3 may be programmed

CURSOR 080000 cursor shift one changed to the right

> 000031 Monday LED flashes

SET DAY	day belonging to first switch time is programmed	SET DAY	Thursday is stored
NEXT	next 'off' time is selected	CURSOR (1x)	last minute of display from address T3 is programmed as a TS on-line basis. If at the first store time the remote displays would be programmed separately as they can be adjusted for every minute.
CURSOR	days Roff so indicate they may be programmed	> (1x)	displaying the > key increments the minutes by 15. Note the off time is programmed too.
> (1x)	Tuesday LED flashes	NEXT	select via (next) on 'off' time
SET DAY	day belonging to off time is stored	CURSOR	days Roff
CURSOR (1x)	hour time Roff	> (1x)	Sunday LED flashes
> (1x)	off time is programmed	SET DAY	Sunday is stored
NEXT	days Roff	CURSOR	hour time Roff
CURSOR	after > is selected for the first time Tuesday must be flash to indicate that the next switches must be on Tuesday or least one in the week	> (1x)	new all switch times are programmed
> (1x)	Wednesday is stored	NEXT	select next switch time
SET DAY	select next 'on' time	CLEAR	the other switch times of T3 are erased as they are not needed. Then the first TS time reappears on the display
CURSOR	hour time Roff	NEXT	by repeatedly depressing the NEXT key all the switch times may be checked. Of the deleted times only the line number and the switch indication are stored
>	off time is programmed	CURSOR (1x)	the user may jump from line to line by setting the cursor to the line number
NEXT	select next 'on' time	> (1x)	In each step the first time of every line appears on the display. The rest of the program may be stopped through with the MODE key
CURSOR	days Roff	CURSOR	the cursor is moved off the display to allow the MODE key to return the processor to the display
> (1x)	Thursday LED flashes	MODE	the time reappears in this display

Memory cards are basically birds of a feather. They all contain memory ICs, BUS buffers and a control circuit. The latter, however, does tend to vary from one system to another. The RAM/EPRQM card described in the September '80 issue was originally designed for use with the SC/MP and 6502 systems, but after a couple of alterations it can be run on the Z80 as well. This involves changing the printed circuit board by breaking 9 tracks and then inserting 7 new wire links. No new components are required. In other words, it is just a 'cut and shunt' exercise.

Figures 1 and 2 show the changes that need to be made to the lower and component overlay sides of the printed circuit board, respectively. As can be seen, very little cutting and linking is required.

memory access and refresh cycles. During normal memory access the CPU starts by outputting addresses. After a short period, the MREQ signal is generated. This is accompanied by the RD strobe during a read cycle, in which case both signals will be synchronous. After the two signals the CPU stops reading data.

Things are different in the write cycle where the CPU produces the MREQ signal and simultaneously transmits the output data to the data bus. But the WD line is not enabled until after a brief interval to allow the active edge of the strobe to be used for data storage (provided the system is buffered in such a way that the data bus really does pass data to memory before the WD strobe arrives!). The WD signal is disabled at the same time as the MREQ signal.

# RAM/EPROM card for the Z80

A. Seul

In principle, the RAM/EPROM card (as published in the Elektor September '80 issue) may be connected to a variety of microprocessors. One or two minor alterations to the control circuit are all that is necessary, in many cases, to match it to a particular system. This article describes the changes needed in order to interface the card to the Z80- and the Z80-A CPU, in particular, as this is introduced elsewhere in the present issue as the 'brain' behind the Polyformant.

## Reasons for the changes

The SC/MP and 6502 systems define both the address range and the direction in which the data transfer is to take place during either the read or write strobe produced by the CPU. In the Z80, on the other hand, a valid address may be output on three separate occasions: during normal memory access, when one of the 256 I/O addresses is being accessed and in the case of memory access during a refresh cycle. Taking into account the additional possibility of a non-valid address, only two CPU lines would seem to be required to define every possible address status. In actual fact, however, the Z80 processor uses three lines:

- MREQ to access memory locations;
- IORQ to access peripheral devices and
- RFSH to access and refresh dynamic RAMs.

Let's forget about IORQ for the moment and see what happens in normal

The memory card may not be accessed during a refresh cycle. What happens here is that the refresh line is enabled first, after which the MREQ signal is strobed. RD and WD are not used, because the CPU ignores data during this particular process.

The control circuit of a memory device operates according to the following parameters:

1. Memory is accessed if MREQ is enabled and RFSH is disabled.
2. Data must be applied to RAM before the WD strobe is enabled.
3. Data must only enter the BUS while RD is enabled and memory is being accessed.

Figure 3 shows the circuit diagram of the modified memory board. The first parameter is met by linking MREQ and RFSH by way of N6 and N7. Pin 8 of N7 will then only go low, if the CPU addresses a memory location. The memory card should only react to a memory access if the relevant memory range is being selected. This is achieved by connecting pin 8 of N7 to pins 18 and 19 of IC5 (the 74154 decoder). Its outputs activate the CS decoder IC6 and IC7 by way of N1 and N2. In addition, the output of N5 produces an active high CARD SELECT signal.

The second requirement is fulfilled by making sure that the card transfers data from the BUS to memory during its quiescent state. Thus, data will also be applied upon the arrival of the WD signal. The 6502 processor implements the WD signal instead of its RD counterpart to transfer data to the data bus when memory is being accessed and the WD signal is disabled. In a Z-80 system, this would go hopelessly wrong: during a write cycle the CARD SELECT signal will precede the WD strobe. The original cir-

1a

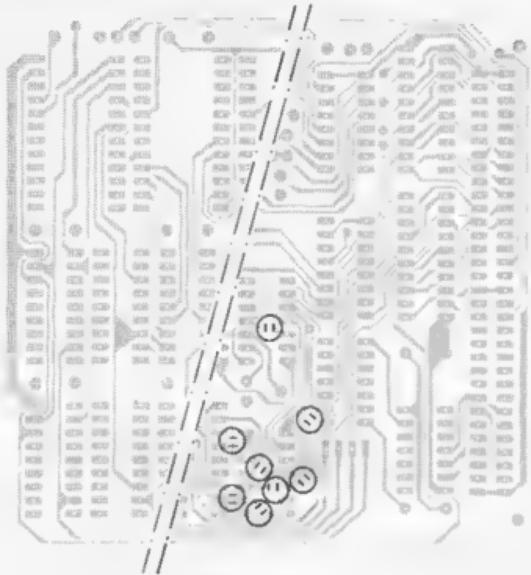


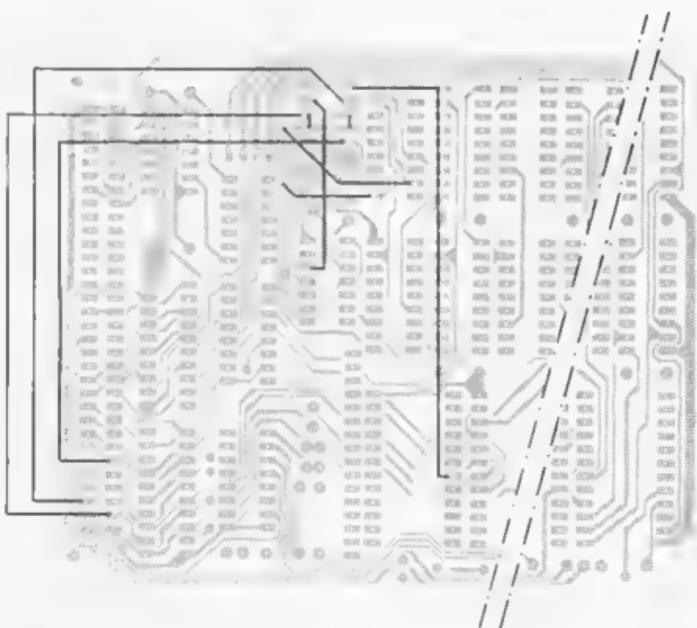
Figure 1a. The circles indicate which tracks on the lower side of the printed circuit board need to be broken.

cuit 'notices' the signals and starts a read cycle. It will therefore transfer RAM data to the BUS until the write pulse  $\overline{WD}$  appears. On the one hand, this prevents data from being applied to RAM upon the arrival of the  $\overline{WD}$  strobe (second parameter) and on the other, the data bus is already being driven by the CPU buffers, as the CPU control circuit has acknowledged the write cycle. Bi-directional transfer is strictly forbidden in the BUS. Depending on which drivers are being operated, current peaks will be produced on the +5 V and GND lines, which could well make the system collapse.

To avoid these problems, the  $\overline{RD}$  signal is inverted by way of N8 (and linked to the CARD SELECT signal by way of N3), and used to control the direction of data transfer in the data bus buffers. N4 serves to buffer the  $\overline{WE}$  line, which has the arduous task of driving 16 ICs.

Inverters N6 and N8 and NAND gate N7 required for the modification are already included on the printed circuit board in IC29 (74LS00). In the original circuit, the unused inputs are either high or low to avoid crosstalk to active gates. These connections should now be replaced by the links indicated in figures 1b and 3. Once all these alterations have been made, the RAM/EPROM card will be ready for use with the Z80. ■

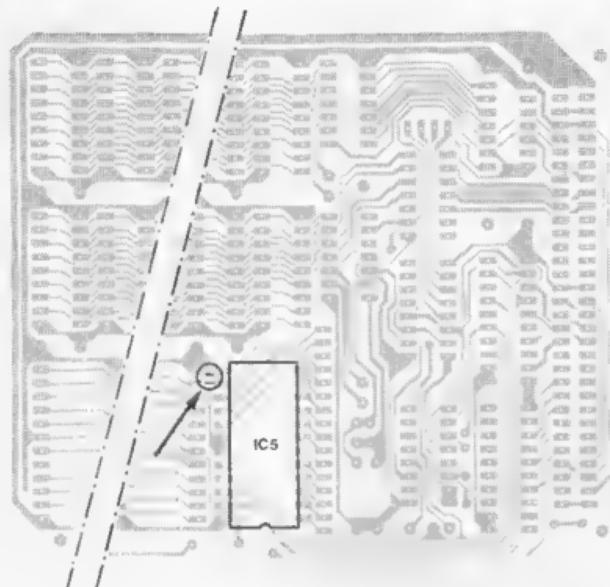
1b



82134-2

Figure 1b. The new wire links on the lower side.

2



82134-3

Figure 2. Only one track needs to be broken on the component overlay side.

3

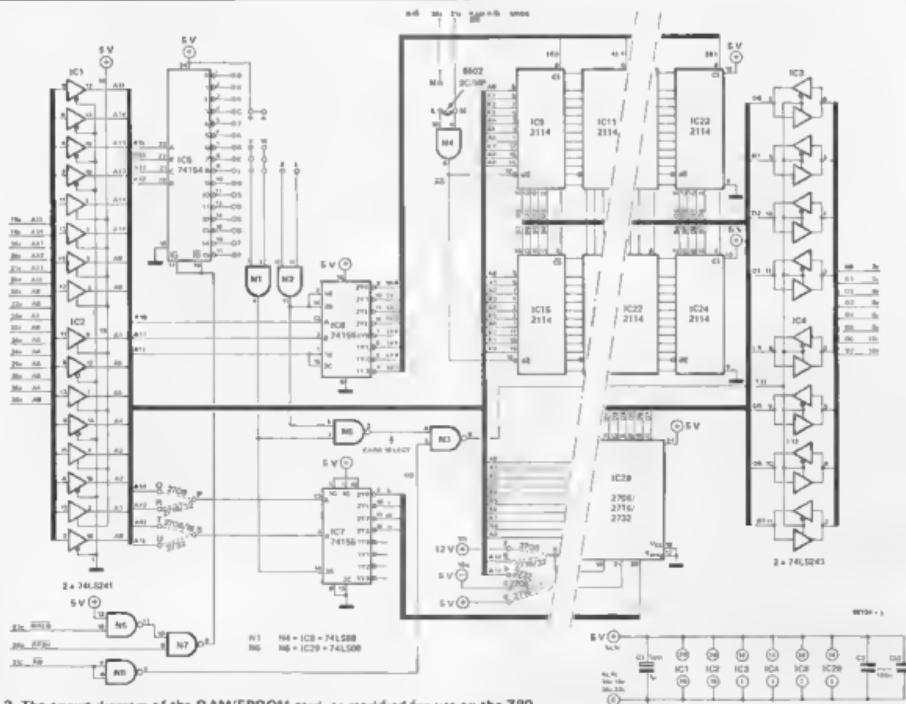


Figure 3. The circuit diagram of the RAM/EPROM card, as modified for use on the Z80.

Junior Computer owners regularly send us programs that they have written for 'their' machine and Elektor's editorial staff dutifully try them all out and 'unravel' them with the disassembler. Unfortunately, the task is not always a rewarding one and occasionally the work resembles that of a pathology lab. Nevertheless, it is gratifying to receive so many sparks of initiative! Any attempt in this direction automatically calls for a disassembler, but that is by no means the only reason for having a 'software cruncher'. Used in combination with the editor and assembler the disassembler enables operators both to write their own programs and decode those gleaned from friends or magazines.

# software cruncher and puncher

**disassemble Junior Computer software  
and program 2716 EPROMs**

Whereas developing one's own software is often like taking a leap in the dark, analysing other people's programs can sometimes be quite a revelation. In either case a disassembler is called for, such as the one described here. In addition, it is a useful aid towards 'BASIC' conversion. And, as the software cruncher is stored in 2716 EPROM, why not include an EPROM programming program, (to use up the remaining EPROM space), together with the EPROM hardware published in January?



## The details

The software cruncher is stored in 2716 EPROM. The software occupies the address range \$F800...\$FFFF. The EPROM may either be mounted on a RAM/EPROM card or on the mini EPROM card published in the April issue. Locations \$F800...\$FDFF store the actual disassembler. \$FDFA...\$FFFF contain the 'EPROM PROGRAMMING UTILITIES' (which are described later on in the article) and \$FFFA...\$FFFF include the vector data with which JC owners are already familiar.

The disassembler section of the software 'cruncher' is shown in Table 1. After initiation (enter the start address \$FC4E through PMI) the computer reports back by defining the relevant function keys. The D key is operated to enter two addresses which 'cord off' the memory range that is to be disassembled (ending in CR). In the

example given in Table 1 this comprises \$0200...\$022F. Note that the end address must be entered and that the 'end address + 1' rule does not apply here.

This is followed by the message 'L, P, SP?'. By depressing the L key the operator can disassemble the entire memory range 'in one go'. The P key, on the other hand, does this in blocks of 15 instructions (a full TV screen, the top line being the last one to be printed before P was operated) and the space bar SP allows each instruction to be disassembled in turn and is therefore the slowest method.

The 'crunched' program in Table 1 gives an idea of the type of information that is printed. Table 2 shows the Hex dump of the disassembler. First of all, the address and the op code of the instruction are displayed followed by the byte(s) contained in the instruction. Then the mnemonics (the instruction 'shorthand') are printed preceded by several spaces. Wherever relevant, the line ends with the operand data. The displacements involved in conditional jump instructions are 'translated', so to speak, as the 'jump address'.

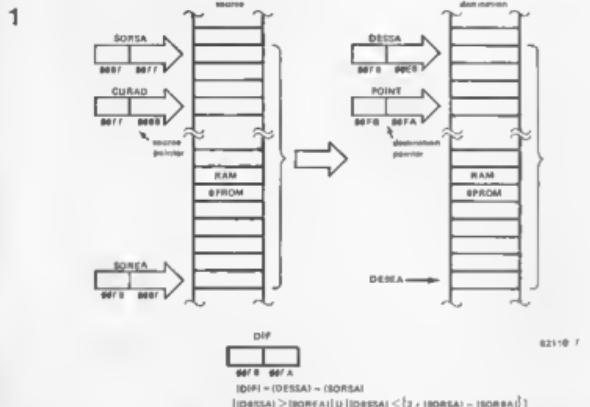
Data that is not acknowledged to be the op code of an instruction has the mnemonic consisting of three American AT symbols assigned to it (see address 021E, for example). Such data is one byte long. Note that FF is not acknowledged as a label op code.

Then R is operated and the program returns to PM. What could be easier?

Table 1.

```
FC4E
FC4E A9 R
VALID COMMANDS: A D H L P R SP
```

D	DISASSEMBLE: 200, 22F
L, P, SP?	L
0200 A9 00	LDA # \$00
0202 AD 01 02	LDA \$0201
0205 A5 03	LDA \$03
0207 A1 04	LDA (\$04,X)
0209 81 05	LDA \$05,Y
020B 85 06	LDA \$06,X
020D 8D 07 08	LDA \$0807,X
0210 89 09 0A	LDA \$0A09,Y
0213 86 0B	LDX \$08,Y
0215 20 0C 0D	JSR \$000C
0218 4C 0E 0F	JMP \$0F0E
021A 6C 10 11	JMP [\$1110]
021E 77	@@@
021F FF	@@@
0220 00	BRK
0221 00	BRK
0222 CA	OEX
0223 C8	INY
0224 E8	INX
0225 OA	ASL A
0226 F0 12	BEQ \$023A
0228 D0 FE	BNE \$0228
022A 80 34	BCS \$0260
022C 90 EE	BCC \$021C
022E FA	@@@
022F 00	BRK



**Figure 1.** The memory ranges involved in the EPRRTL routine. Operating the M, R, V or F key causes the CURAO and POINT pointers to move through every location from SORSA and QESEA to SOREA and QESEA, respectively.

As for the H and A keys, depressing H is equivalent to operating M during PM and A represents 'ASCII dump'. Thus, a hex dump is printed after two address entries followed by CR (see table 2). The A key causes a hex dump to be printed showing the ASCII code of any alphanumeric character within the \$20...\$7E range. In the case of data outside this range, a space appears. This feature allows data, such as computer messages that need printing, to be located swiftly. Once readers manage to crunch the disassembler they will see that this is riddled with such messages.

Not only but also . . .

The printing operation of the dump or listing may be interrupted by depressing the BRK key. The BRK jump vector leads the 6502 µP to a central point in the program where it waits for a (new) key to be pressed.

When two addresses are entered for the purpose of defining a listing or dump, the second address must be higher than the first. Otherwise, the two addresses will have to be re-entered, only this

time in the right order please! As well as storing date in much used memory locations in pages 00 and 1A, the software cruncher must dispose of \$0010 . . . \$0027. \$0028 must now also be added to accommodate the extra software. Operators must be careful not to use these memory locations for the program they wish to 'sort out'.

## Software evaluation

**Software puncher**  
As mentioned earlier, now that we have the necessary hardware (Elektor January 1982), a start can be made on loading RAM or EPROM software into 2716s. The program is started by

way of PM at address \$FDDA. After initialisation, the name of the program is printed along with a list of valid keys. Then the *parameter key*, *P*, should be depressed so as to define the address range by entering three addresses, as shown in figure 1. First of all, the 'FIRST, LAST SOURCE ADDRESS' must be specified, in other words, the SORSA and SOREA addresses at either end of the data block that is to be stored or relocated. Make sure SOREA has a higher number than SORSA, especially otherwise the entry procedure (first address - comma - last address - CR) will have to be repeated. Next, enter the 'FIRST DESTINATION ADDRESS'. This is known as DESSA and determines the location of the first address belonging to the data being programmed or moved. (Enter the first address followed by CR.)

The following key functions are valid:  
**The M (MOVE) key** ensures that the SOSEA...SOREA data block is stored or relocated (provided the EPROM programmer is connected and prepared for programming — more about this later) into the destination block DESEA...DESEA. For reasons involving the V key, the two blocks may not overlap. The three address pointers must be set according to the parameters indicated in figure 1. At the end of the program 'DATA MOVED' appears on the screen as a reminder.

The F (FF check) key enables the operator to check whether locations DESSA...DESSA+n-1 contain FF (n represents the number of memory locations in the data block being programmed). If so, data may be stored in that particular range. The address and contents of any memory locations that do not contain FF are printed. Once all 'n' locations have been run through, 'DATA COMPARED' appears.

The **R (RELOCATE)** key. All the absolute addresses within the data block SORSA... SOREA are adapted to the new situation brought about by moving or programming a data block. The new address is determined by the contents of DIF (see figure 1). At the end of the procedure, 'RELOCATED' is printed. The R key function is not needed while relocatable software is being stored (without any internal JMPs and subroutines) or if the contents of one EPROM are being loaded into another. In order to copy RAM data into EPROM, depress R, then M. But to store EPROM data into RAM, depress M followed by R.

The **V (VERIFY)** key. This compares the original data block and its relocated version, byte by byte. Whenever an error crops up, the offending location is printed along with its address and constants. The operation signs off with the 'DATA COMPARED' message.

The **B (BACK)** key introduces a return to PM whenever the computer is ready or the operator wishes to disassemble a relocated/programmed data block (to verify the R key routine).

The **ST key (ST/NMI on the main keyboard)** allows a return to take place from PM to EPRUTL, like a warm start entry. Then 'XXXX < AD = < YYYY TO > ZZZZ' appears, where XXXX stands for the FIRST SOURCE ADDRESS, YYYY stands for the LAST SOURCE ADDRESS and ZZZZ stands for the FIRST DESTINATION ADDRESS.

By the way, ST may also be operated during EPRUTL to print the three address parameters and their interim status during an operation. This is extremely useful, as sometimes the parameters need to be temporarily altered. At the same time, the operator is reminded of what was entered three 'screenfuls' before.

## How to prevent programs from going 'off the rails'

1. The EPROM programmer must be connected to the bus board. The card is addressed in the normal manner during programming. This means that a 'FIRST DESTINATION ADDRESS' (\$2000 or higher) must be entered for reasons described in *Box 3*. But this does not imply that any EPROM data located below \$2000 in the memory map, such as the main board monitor and the TM and PM software, is excluded. Details are provided in point 3.

2. Using the S3...S6 switches, a 4K address block must be selected that does not coincide with any existing data blocks. Otherwise double addressing occurs. If necessary, remove one or two memory cards from the bus board for the time being. Remember that the first two 4K blocks are also out of bounds (see point 1).

3. The FIRST DESTINATION ADDRESS entered just before the start of the program must be located within the selected 4K block (see point 2). This address does not necessarily have to be the ultimate first address (it may be modified later). Right now we intend to load data into the EPROM on the programmer, byte by byte, with the aid of the M key. But take heed! If any absolute addresses need to be altered, start by entering the real FIRST DESTINATION ADDRESS using the P key. (Then depress R and P again, followed by the first address of the EPROM programmer.) Finally, operate M.

4. S2 on the EPROM programmer is not switched 'on' until just before the actual programming sequence (with the M key). During programming LED D9 lights and remains lit for the entire process. (About 20 bytes are loaded per second, so it takes quite a while). S2 should be switched off as soon as D9

has gone out and 'DATA MOVED' appears on the screen!

5. 2716 and 2732 EPROMs have one thing in common: they do not enjoy being exposed to the full brunt of the 25 V programming voltage without having the comforting protection of the 5 V supply voltage. The circuit in figure 2 is added to the EPROM programmer hardware to cushion the blow.

6. To find out whether a 2716 IC is truly empty, access a 4K block on the EPROM programmer; select a FIRST DESTINATION ADDRESS that either corresponds to the first address in the range or to one 2048 locations further on, and enter any 2K data block. Now depress the F key.

7. Whenever EPROM software needs to be duplicated, store the 'master' version on a RAM/EPROM card, (unless it is a system EPROM). Insert the (presumably) empty EPROM on the programmer board. Then follow the instructions given in points 3 and 4. After a short while the data 'transfusion' should be complete.

8. Loading EPROM software into RAM is no problem and may come in handy whenever system programs are to be stored on cassette or the contents of an EPROM are to be changed. First copy the data (using the M key) and then relocate it (with the R key), if necessary. The V key allows the operator to check which locations have been altered as a result of the R key routine.

9. When using the R key, watch out for look-up tables and 'strings'. Data such as '20 41 54' is ambiguous, for it may either be the ASCII code for 'WAT', or stand for JSR-\$5441! If 54 constitutes an ADH within the data block being programmed (\$2000...\$5FFF on the dynamic RAM card) the chances are, operating the R key will cause the 54 to be deleted. That is why it is a good idea to check the location of such tables beforehand, and make sure they remain intact after R is depressed (before M is operated). The disassembler is of great help in these matters.

10. A special program, as described in the January article on EPROM software, would be needed to store data in the 'step' mode using the original monitor routine. Fortunately, this is no longer necessary, thanks to the PM routine. Just enter the EPROM location to be programmed (the EPROM programmer version see point 3), depress the space bar, enter the data and press the '.' key. Make sure the EPROM programmer is ready for programming, as indicated in point 4.

Although very few keys are needed to program EPROMs, operators will discover that they offer a surprisingly versatile repertoire.

## 2

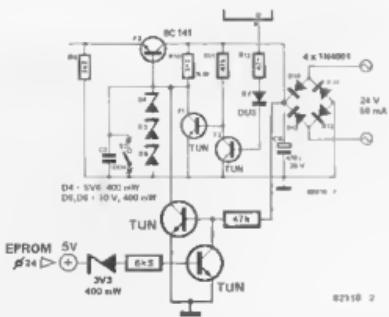


Figure 2. This circuit is added to the EPROM programmer to prevent the EPROM being loaded from becoming a fried chip if S2 is inadvertently switched on before the EPROM programmer power supply is connected up. A common mains switch does not provide a 100% guarantee!

We are informed that a suitably programmed 2716 will be available from Technomatic Ltd, London.

# market

## 'Small business' printer

The latest family of bi-directional logic seeking dot matrix printers from Centronics Ltd — the 150 series — is now being stocked by Bytech Limited. These versatile 150 character per second machines are available for either 10-inch or 15-inch paper widths, and have snap-on tractors to handle roll, cut-sheet or fan-fold paper.



The series, which comes complete with a time-saving cassette ribbon system, features a 96 ASCII character set, plus an optional international character set. Printing may be carried out in 40, 80 or 132 column format, using a 100% duty cycle. A self testing facility and cover safety interlock complete the relatively sophisticated functions offered, and both types are available with either serial or parallel interfaces.

**Bytech Limited,**  
Unit 57, Suttons Ind. Park,  
London Road,  
Earley,  
Reading,  
Berks,  
Telephone: 0734-61031

(2348 M)

a time access control for oscilloscopes or pen recorders.

Up to five frequency decades can be covered in a single sweep with automatic sweep times being internally selected from 0.1 to 100 seconds both continuous and single to match the application. The single sweep mode can also be controlled manually from the front panel or sweep speeds determined by external signals. Automatic sweep speed compensation has been provided to maintain a constant sweep time period for any arbitrarily set width. The WG 230 is neat and compact, measuring 128 (W) x 190 (H) x 285 (D) mm and weighing approximately 4.2 kg.

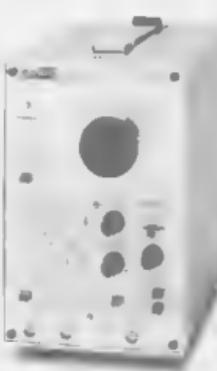
**House of Instruments,**  
Clifton Chambers, 62,  
High Street,  
Saffron Walden,  
Essex CB10 1EE  
Telephone: 0799-24922

without re-tooling of the existing panel. Illumination is provided by either neon or incandescent lamps through red, green and amber actuator buttons whilst the non-illuminated thermoplastic buttons are available in red, white and black. Both types can be hot stamped in red, white and black, with legends to customers' specifications.

**Pushette switches** have a 125 V AC/28 V DC rating of up to 10 amps 250 V AC and models are available for low voltage DC applications.

**N.S.F. Limited,**  
Keighley,  
West Yorkshire BD21 5EF,  
Telephone: 0535-61144

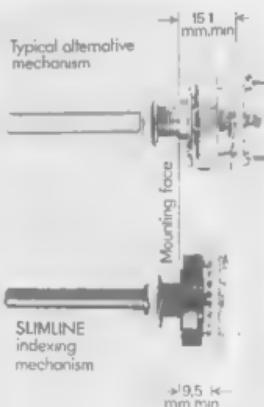
(2341 M)



(2345 M)

## Slimline wafer switch

Where behind panel dimensions are critical, especially in applications incorporating printed circuit rotary wafer switches, the new Slimline mechanism provides a smooth, efficient and positive indexing, all in a slender package. Being a 'ready finished' component, the all moulded construction gives protection against corrosion and requires no additional lubrication. The swing in length, compared with existing alternative models, is approximately 5 mm to the first start. With 30 and 36 degree indexing available, the switching



ranges from 1 pole, 2 to 12 ways up to 6 poles, 2 ways per wafer, and the 12 or 14 pin terminations of the PCA stator board are positioned conveniently along one edge for easy attachment to printed circuit boards.

**N.S.F. Limited,**  
Keighley,  
West Yorkshire BD21 5EF.  
Telephone: 0535-61144

(2336 M)

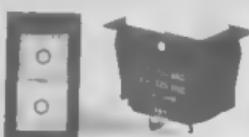
## Combined function, sweep and pulse generator

House of Instruments announce the WG 230 from Trio, which combines the capabilities of a function, sweep and pulse generator in one high quality compact unit. The wide frequency bandwidth is covered by a log and linear divided, high resolution main dial from 20 Hz to 200 kHz, with an auxiliary control covering the range 2 Hz to 20 Hz.

Four main types of outputs are available: sine, square, triangle and TTL level pulse. Output impedance is 600 ohms with 7 V rms sine and 10 V pp for square and triangle controlled by 60 dB of switched and 20 dB of variable attenuation. Flatness is better than 0.2 dB making the WG 230 ideal in determining frequency characteristics. The TTL pulse output can be used to drive logic circuitry or act as a clock source substitute. FM modulation, another convenient feature when measuring frequency characteristics over a specific band, is available via an external signal. External DC can be used for VCO applications while a useful sweep ramp output is provided for use as

## Pushette switches

A new line of pushbutton switches is now available from N.S.F. Limited. Standard features of the Pushette switches include illuminated and non-illuminated buttons, interlocking buttons, solder lug, spade and screw terminal, maintained and momentary circuits, bezels and two methods of snap-in mounting. The new pushbutton switches are interchangeable with standard snap-in rocker switch models, thus using the same panel cut-outs and so can be substituted



# market

# GAMES COMPUTER BOOK

**an exciting  
introduction to  
microprocessors**



The first acquaintance with microprocessors can be rather frightening. You are not only confronted with a large and complex circuit, but also with a new language: 'bytes', 'CPU', 'RAM', 'peripherals' and so on. Worse still, the finished article is a miniature computer and so you have to think up some sufficiently challenging things for it to do! This book provides a different — and, in many ways, easier — approach.

The TV games computer is dedicated to one specific task: putting an interesting picture on a TV screen, and modifying it as required in the course of a game. Right from the outset, therefore, we know what the system is intended to do. Having built the unit, 'programs' can be run in from a tape: adventure games, brain teasers, invasion from outer space, car racing, jackpot and so on. This, in itself, makes it interesting to build and use the TV games computer.

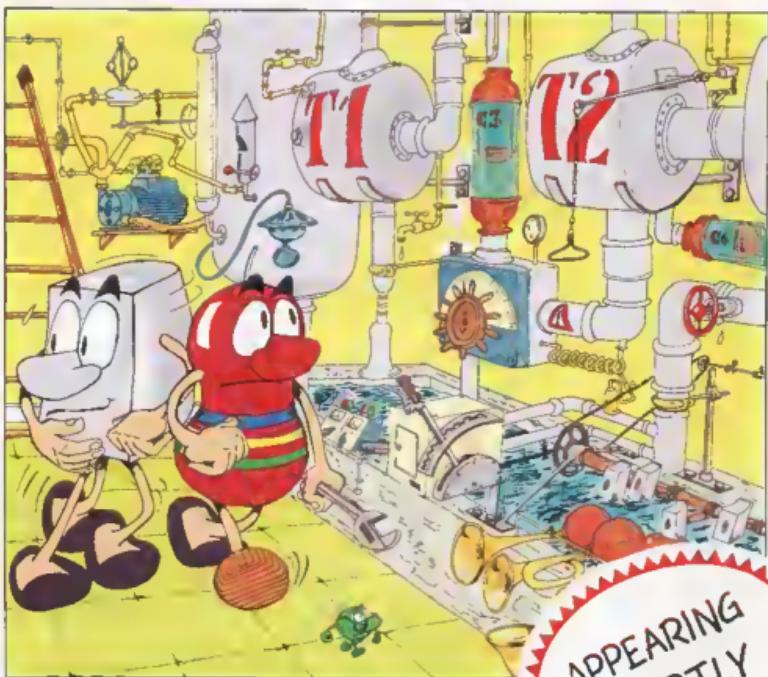
There is more, however. When the urge to develop your own games becomes irresistible, this will prove surprisingly easy! This book describes all the component parts of the system, in progressively greater detail. It also contains hints on how to write programs, with several 'general-purpose routines' that can be included in games as required. This information, combined with 'hands-on experience' on the actual unit, will provide a relatively painless introduction into the fascinating world of microprocessors!

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